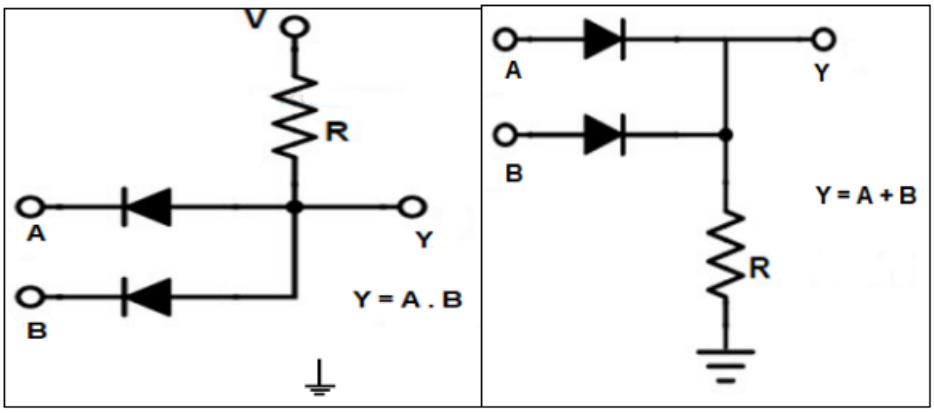
DTE MSBTE PAPERS
2 MARKS QUESTIONS
(WINTER-18)

1.Write the radix of binary, octal, decimal and hexadecimal number system.
Ans: Radix of: Binary – 2
Octal – 8
Decimal – 10
Hexadecimal -16

2.Draw the circuit diagram for AND and OR gates using diodes.
Ans: Diode AND gate : Diode OR gate :



3. Write simple example of Boolean expression for SOP and POS.
Ans: SOP form:

$$Y = AB + BC + A\bar{C}$$

POS form:

2

$$Y = (A + B)(B + C)(A + \overline{C})$$

4. State the necessity of multiplexer. **(write any two proper points)**

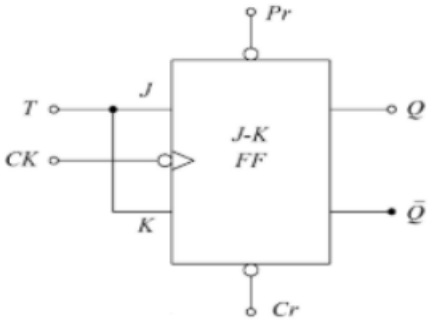
Ans: Necessity of Multiplexer:

- It reduces the number of wires required to pass data from source to destination.
- For minimizing the hardware circuit.
- For simplifying logic design.
- In most digital circuits, many signals or channels are to be transmitted, and then it becomes necessary to send the data on a single line simultaneously.
- Reduces the cost as sending many signals separately is expensive and requires more wires to send.

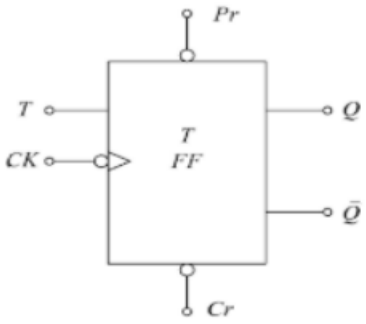
5. Draw logic diagram of T flip-flop and give its truth table.

Ans: **Note**: Diagram Using logic gates with proper connection also can be consider.

Logic Diagram:



OR



Truth Table:

3

Input T_n	Output Q_{n+1}	Operation Performed
0	Q_n	No change
1	$\overline{Q}_n$	Toggle

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6. Define modulus of a counter. Write the numbers of flip flops required for Mod-6 counter.

Ans:

- Modulus of counter is defined as number of states/clock the counter countes.
- The numbers of flip flops required for Mod-6 counter is 3.

7. State function of preset and clear in flip flop.

Ans:

- In the flip flop, when the power is switched on, the state of the circuit is uncertain i.e. may be Q = 1 or Q = 0.
- Hence, the function of preset is to set a flip flop

i.e Q = 1 and the function of clear is to clear a flip flop i.e. Q = 0.

Inputs			Output	Operation performed
CK	*Cr*	*Pr*	*Q*	
1	1	1	Q_{n+1} (Table 7.1)	Normal FLIP-FLOP
0	0	1	0	Clear
0	1	0	1	Preset

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(SUMMER-18)

1. List the binary, octal and hexadecimal numbers for decimal no. 0 to 15.

Ans:

DECIMAL	BINARY	OCTAL	HEXADECIMAL
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

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2. Define fan-in and fan-out of a gate.
Ans: Fan-in is a term that defines the maximum number of digital inputs that a single logic gate can accept. Most transistor-transistor logic (TTL) gates have one or two inputs, although some have more than two. A typical logic gate has a fan-in of 1 or 2.
Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed. Most transistor-transistor logic (TTL) gates can feed up to 10 other digital gates.

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3. State two specification of DAC.

Ans:

1. Resolution: Resolution is defined as the ratio of change in analog output voltage resulting from a change of 1 LSB at the digital input VFS is defined as the full scale analog output voltage i.e. the analog output voltage when all the digital input with all digits 1. Resolution = VFS /(2n −1)
2. Accuracy: Accuracy indicates how close the analog output voltage is to its theoretical value. It indicates the deviation of actual output from the theoretical value. Accuracy depends on the accuracy of the resistors used in the ladder, and the precision of the reference voltage used. Accuracy is always specified in terms of percentage of the full scale output that means maximum output voltage
3. Linearity: The relation between the digital input and analog output should be linear. However practically it is not so due to the error in the values of resistors used for the resistive networks.
4. Temperature sensitivity: The analog output voltage of D to A converter should not change due to changes in temperature. But practically the output is a function of temperature. It is so because the resistance values and OPAMP parameters change with changes in temperature.
5. Settling time: The time required to settle the analog output within the final value, after the change in digital input is called as settling time. The settling time should be as short as possible.
6. Long term drift long term drift is mainly due to resistor and semiconductor aging and can affect all the characteristics. Characteristics mainly affected are linearity, speed etc.
7. Supply rejection Supply rejection indicates the ability of DAC to maintain scale, linearity and other important characteristics when the supply voltage is varied. Supply rejection is usually specified as percentage of full-scale change at or near full scale voltage at 25oe
8. Speed: It is defined as the time needed to perform a conversion from digital to analog. It is also defined as the number of conversions that can be performed per second.

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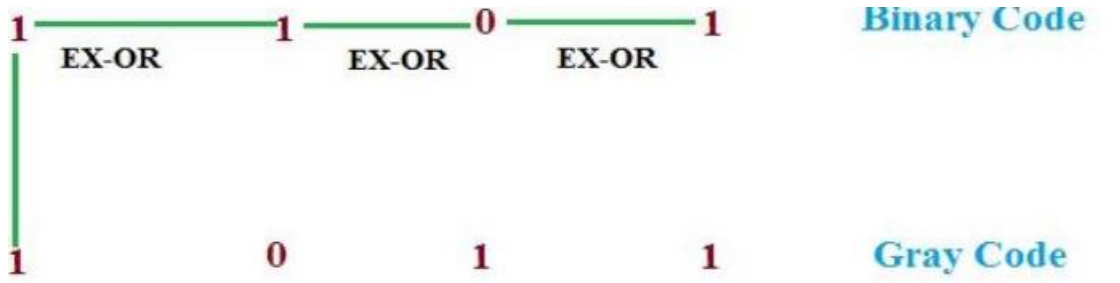
4. Compare between synchronous and asynchronous counter. **(any two points)**
Ans:

Synchronous Counter	Asynchronous Counter
All flip flops are triggered with same clock.	Different clock is applied to different flip flops.
It is faster.	It is lower
Design is complex.	I Design is relatively easy.
Decoding errors not present.	Decoding errors present.
Any required sequence can be designed	Only fixed sequence can be designed.

5. Write the Gray code to given no.(1101)2 =(?) Gray.
Ans:



$(1101)_2$ = (1011) Gray

6. Define encoder, write the IC number of IC used as decimal l to BCD encoder.
Ans: An encoder is a device or circuit that converts information from one format or code to another, for the purpose of standardization, speed or compression.
Decimal to BCD encoder IC- 74147.

7.Draw the logical symbol of EX-OR and EX-NOR gate.
Ans:

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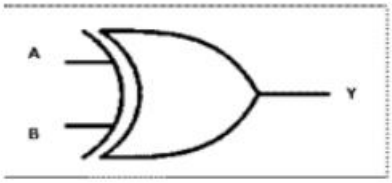
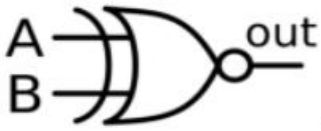
EX-OR GATE:-



$A \cdot \overline{B} + \overline{A} \cdot B$

EX-NOR GATE:-



$A \cdot B + \overline{A} \cdot \overline{B}$

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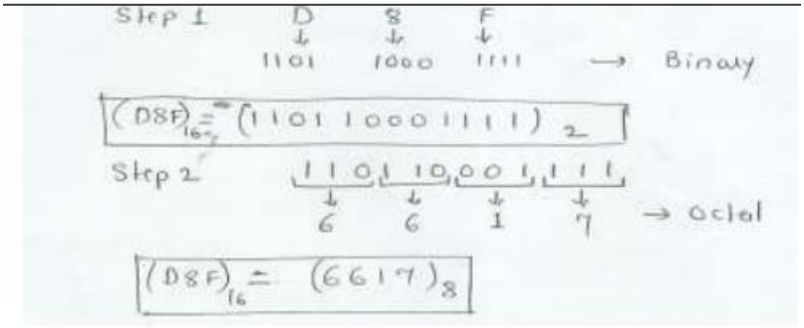
(WINTER-19)

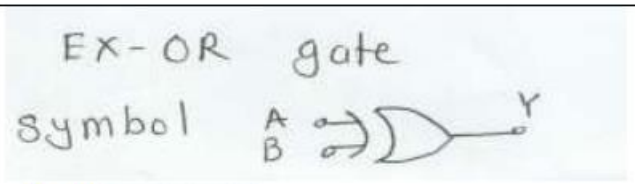
1. Convert (D8F) 16into binary and octal.

Ans:



2. Draw symbol, Truth table and logic equation of Ex-OR gate.

Ans:



Logic Equation = $A\bar{B}+\bar{A}B$ OR $A \oplus B$

Truth Table:

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

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3. State the De Morgan's Theorems.

Ans:

De Morgan's 1st Theorem complement of sum is equal to product of their individual complements.

$\overline{A+B} = \overline{A} \bullet \overline{B}$

De Morgan's 2nd theorem Complement of product is equal to sum of their individual complements.

$\overline{A \bullet B} = \overline{A} + \overline{B}$

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4. Convert the following expression into standard SOP form.

$Y = AB + A\bar{C} + BC$

Ans:

$Y = AB + A\bar{C} + BC$

Total variable ABC

1st Product term = AB (C is missing)

2nd Product term = $A\bar{C}$ (B is missing)

3rd Product term = BC (A is missing)

$Y = AB \bullet 1 + A\bar{C} \bullet 1 + BC \bullet 1$

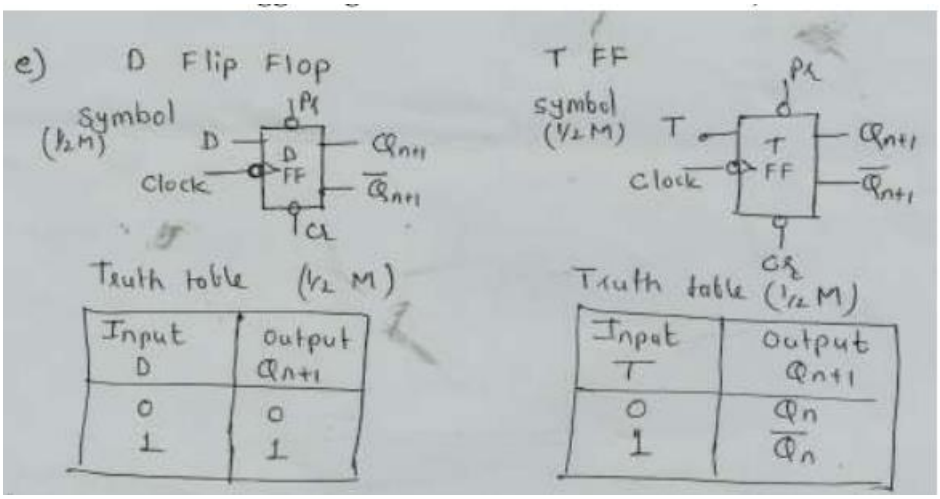
$Y = AB(C+\bar{C})\ A\bar{C}(B+\bar{B}) + BC(A+\bar{A})$

$Y = \underline{\underline{ABC}} + \underline{AB\bar{C}} + \underline{AB\bar{C}} + A\bar{B}\bar{C} + \underline{\underline{ABC}} + \bar{A}BC$ $(\because A+\bar{A} = A)$

$Y = ABC + AB\bar{C} + A\bar{B}\bar{C} + \bar{A}BC$ Standard SOP Form

5. Draw symbol and write truth table of D and T Flip Flop.

Ans: **(Note: Symbol with other triggering method also can be consider)**



6. Write down number of flip flops are required to count 16 clock pulses.

Ans: No of states= no. of clock pulses = 16

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$2^n = m$
n = no.of flip flops requried
m= no.of states
$2^n = 16$
n = 4
4 flip flops are required to count 16 clock pulse.

7. List the types of DAC.
Ans: 1) Binary weighted DAC.
2) R –2R ladder network DAC.

(SUMMER-22)

1. Convert $(1101011)_2 = (\quad)_{16}$ and
$(1111011)_2 = (\quad)_8$

Ans:

a. First, convert 1101011_2 into decimal, by using above steps:

$= 1101011_2$

$= 1 \times 2^6 1 \times 2^5 0 \times 2^4 1 \times 2^3 0 \times 2^2 1 \times 2^1 1 \times 2^0$

$= 107_{10}$

Now, we have to convert 107_{10} to hexadecimal

107 / 16 = 6 with remainder 11 i.e. (B)
6 / 16 = 0 with remainder 6

Then just write down the remainders in the reverse order to get the answer, The binary number 1101011 converted to hexadecimal is therefore equal to : **6B**

b. First, convert 1111011_2 into decimal, by using above steps:

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$= 1111011_2$

$= 1 \times 2^6 1 \times 2^5 1 \times 2^4 1 \times 2^3 0 \times 2^2 1 \times 2^1 1 \times 2^0$

$= 123_{10}$

Now, we have to convert 123_{10} to octal

123 / 8 = 15 with remainder 3
15 / 8 = 1 with remainder 7
1 / 8 = 0 with remainder 1

Then just write down the remainders in the reverse order to get the answer, The binary number 1111011 converted to octal is therefore equal to : **173**

2. List triggering methods used for triggering flip flops.

Ans: a. Negative edge triggering.
b. Positive edge triggering.

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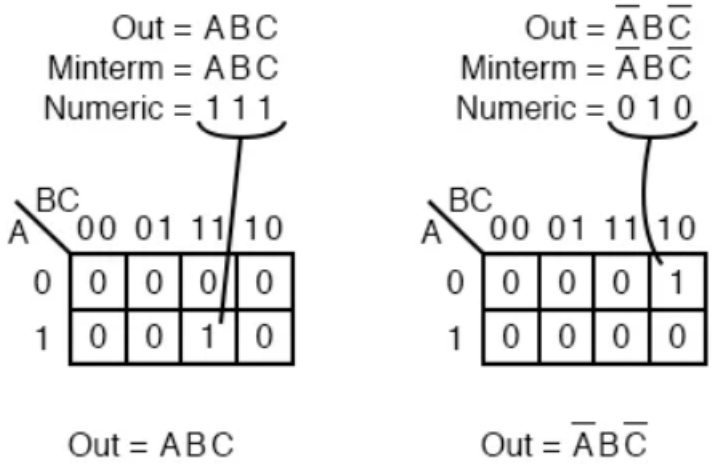
3. Define Minterm and Maxterm w.r.t. K-map.

Ans: We perform the Sum of minterm also known as Sum of products (SOP).

● The minterm for each combination of the variables that produce a 1 in the function and then taking the OR of all those terms.

We perform the Product of Maxterm also known as Product of sum (POS).

● The maxterm for each combination of the variables that produce a 0 in the function and then taking the AND of all those terms.



4. Define shift register and list its types.

Ans: Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses.

There are four types of shift register:

a. Serial In Serial Out shift register (SISO)
b. Serial In parallel Out shift register (SIPO)
c. Parallel In Serial Out shift register (PISO)
d. Parallel In parallel Out shift register (PIPO)

5. List any two specifications of IC-DAC 0808.

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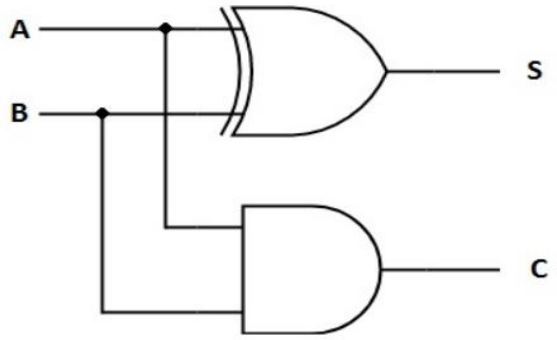
Ans:

- Relative exactness at ±0.19% highest error.
- The range of voltage power supply will be ±4.5V to ±18VN.
- Noninverting digital i/PS are compatible with CMOS & TTL.
- The settling time is very fast 150 ns.
- Highest power dissipation will be 1000 mW.

6. Draw logical circuit diagram of half adder circuit.

Ans:



SUM S = A+B

CARRY C = A.B

7. Write truth table of D type flip-flop.

Ans:

clk	Input D_n	Output Q_{n+1}
↓	0	0
↓	1	1

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(WINTER-22)

1. Write radix of binary, octal, hexadecimal number system.

Ans:

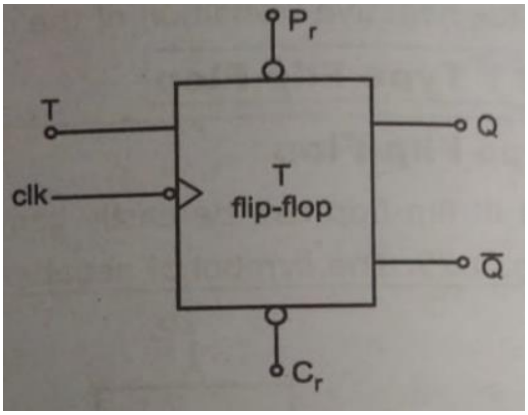
decimal system has a radix of 10
octal system has a radix of 8
hexadecimal is radix 16
binary radix 2.

2. State necessity of demultiplexer.

Ans: Demultiplexers are used in digital control systems to select one signal from a mutual stream of signals. Demultiplexers are also employed for data transmission in synchronous systems. Demultiplexers are also utilized in data acquisition systems.

3. Draw symbol and write the truth table for T-flipflop.

Ans:



clk	Input T_n	Output Q_{n+1}
↓	0	Q_n
↓	1	$\overline{Q}_n$

SYMBOL **TRUTH TABLE**

4. Compare between synchronous and asynchronous counter.

Ans:

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Sr. No.	Parameter	Asynchronous counter	Synchronous counter
1.	Circuit complexity	Logic circuit is simple.	With increase in number of states, the logic circuit becomes complicated.
2.	Connection pattern	Output of the preceding FF, is connected to clock of the next FF.	There is no connection between output of preceding FF and CLK of next one.
3.	Clock input	All the FFs are not clocked simultaneously.	All FFs receive clock signal simultaneously.
4.	Propagation delay	P.D. = n * (td) where n is number of FF and td is p.d. per FF.	P.D. = n * (td)FF + (td)gate. It is much shorter than that of asynchronous counter.
5.	Maximum frequency of operation	Low because of the long propagation delay.	High due to shorter propagation delay.

5. Write Gray code to given number (11111)2 = (?)Gray.

Ans: Binary Code : 11111

Gray Code : 10000

6. State two features of ADC IC0809.

Ans: The ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications.

7. Draw four variable K-map.

Ans:

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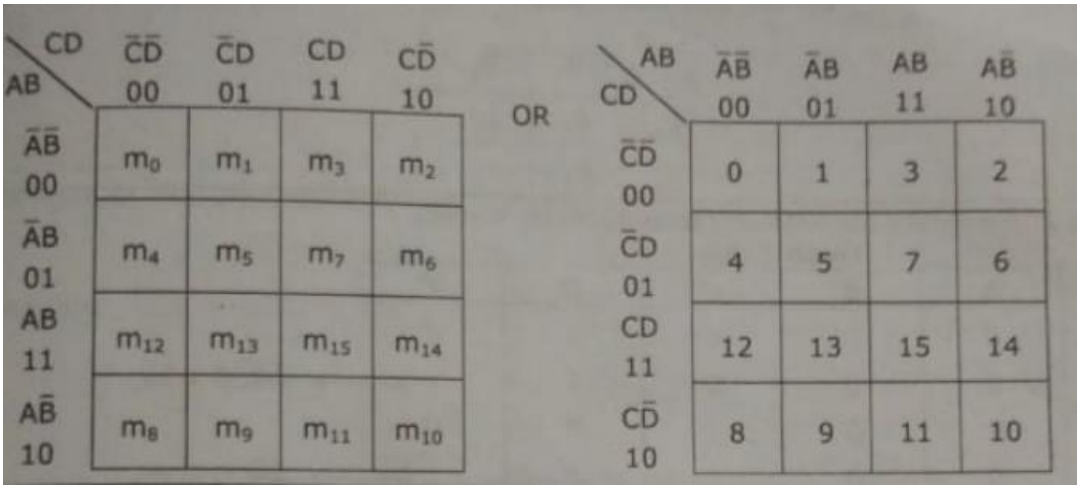

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	m_0	m_1	m_3	m_2
$\bar{A}B$ 01	m_4	m_5	m_7	m_6
AB 11	m_{12}	m_{13}	m_{15}	m_{14}
$A\bar{B}$ 10	m_8	m_9	m_{11}	m_{10}

OR

CD \ AB	$\bar{A}\bar{B}$ 00	$\bar{A}B$ 01	AB 11	$A\bar{B}$ 10
$\bar{C}\bar{D}$ 00	0	1	3	2
$\bar{C}D$ 01	4	5	7	6
CD 11	12	13	15	14
$C\bar{D}$ 10	8	9	11	10

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DTE MSBTE PAPERS
4 MARKS QUESTIONS
(WINTER-18)

1. Draw the block diagram of Programmable Logic Array.

Ans: Diagram: -

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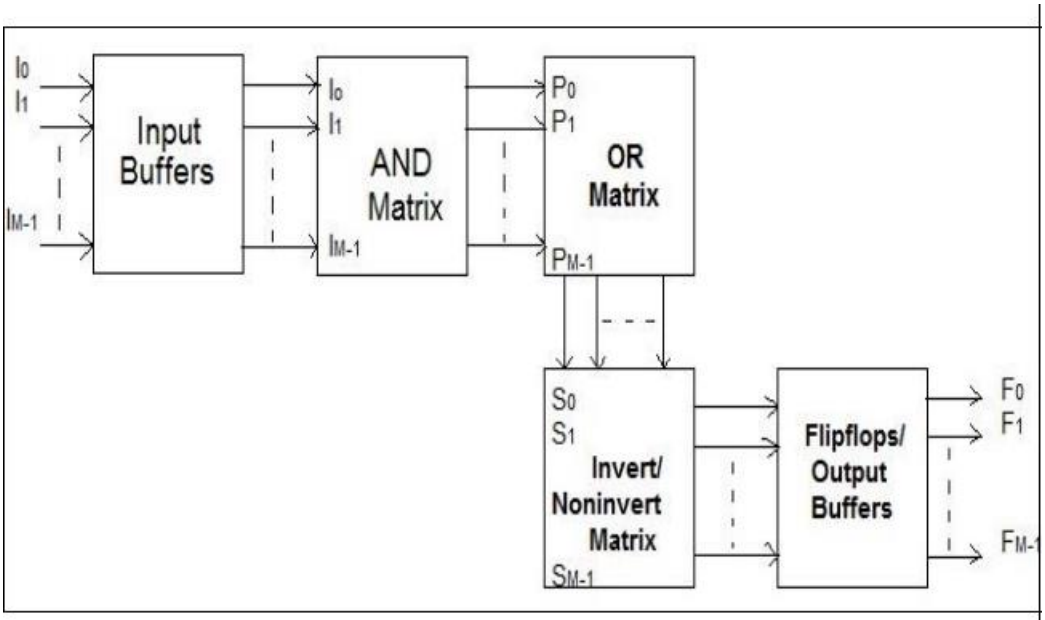
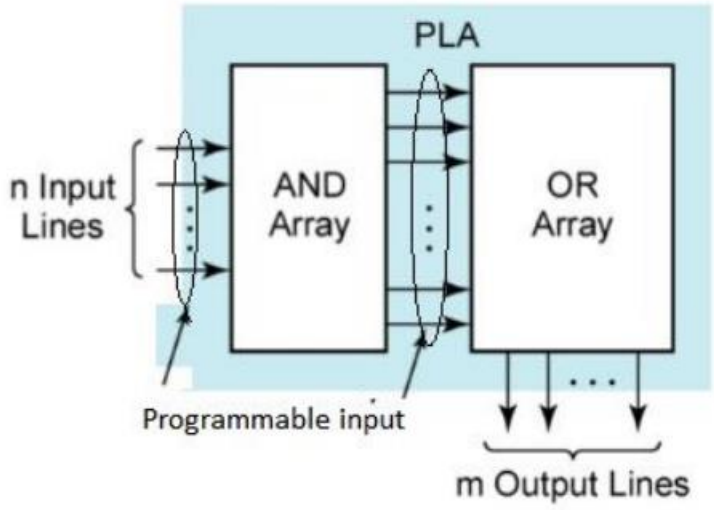


Block diagram of Programmable Logic Array

OR



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2. **Convert –**
$(255)_{10} = (?)_{16} = (?)_8$
$(157)_{10} = (?)_{BCD} = (?)_{Excess3}$

Ans:

(i) $(255)_{10} = (FF)_{16} = (377)_8$

$(255)_{10} = (FF)_{16}$

16 | 255	F (15)	↑
15	F	

$(255)_{10} = (377)_8$

8 | 255	7	↑
8 | 31	7	
3	3	

(ii) $(157)_{10} = (000101010111)_{BCD} = (010010001010)_{Excess3}$

$(157)_{10} = (000101010111)_{BCD}$

1 5 7
0001 0101 0111

$(000101010111)_{BCD} = (010010001010)_{Excess3}$

```
  1 1   1 1 1   1 1 1
  0001  0101  0111
+ 0011  0011  0011
  0100  1000  1010
```

3. Draw the symbol, truth table and logic expression of any one universal logic gate. Write reason why it is called universal gate.
Ans: **(Note: Any one universal gate has to be considered.)**

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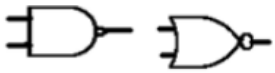
Universal Gates: NAND or NOR Symbol:



Truth table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Logic expression:

$Y = \overline{A \cdot B}$ $Y = \overline{(A + B)}$

NAND and NOR gates are called as “Universal Gate” as it is possible to implement any Boolean expression using these gates.

4. Minimize the following expression using K-Map. ƒ(A, B, C, D) = ∑m (0, 1, 2, 4, 5, 7, 8, 9, 10)

Ans:

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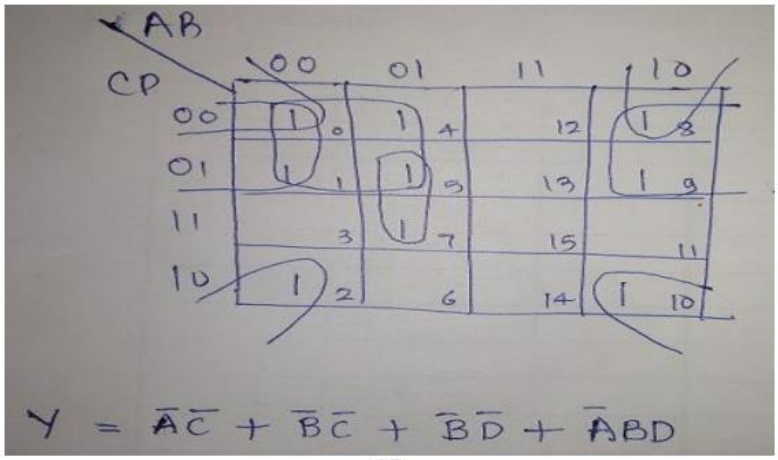

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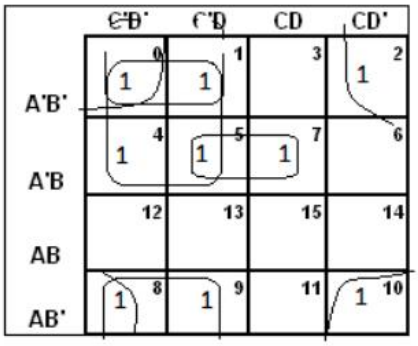

$\bar{A}\bar{C} + \bar{B}\bar{C} + \bar{B}\bar{D} + \bar{A}BD$

5. Compare TTL and CMOS logic families on the basis of following:

(i) Propagation delay

(ii) Power Dissipation

(iii) Fan-out

(iv) Basic gate

Ans: **NOTE: - (Relevant points of comparison- 1 M for each point)**

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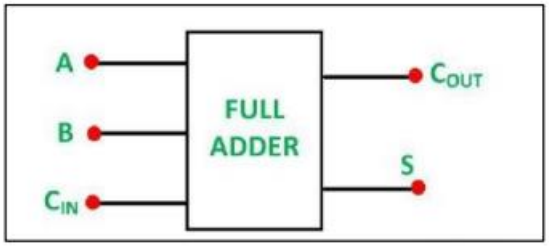
Parameter	CMOS	TTL
Propagation delay	70-105 nsec/more than TTL	10 nsec/Less than CMOS
Power Dissipation	Less 0.1 mW/Less than TTL	More 10 mW/ More than CMOS
Fan-out	50/More than TTL	10/Less than CMOS
Basic gate	NAND/NOR	NAND

6. Describe the function of full Adder Circuit using its truth table, K-Map simplification and logic diagram.

Ans: **(Diagram- 1M, Truth table-1M, K-map- 1M, Logic diagram-1 M)**

A full adder is a combinational logic circuit that performs addition between three bits, the two input bits A and B, and carry C from the previous bit.

Block diagram:



Truth Table:

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Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K Map:

For Carry (C_{out})

A \ BC_{in}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$C_{out} = AB + A C_{in} + B C_{in}$

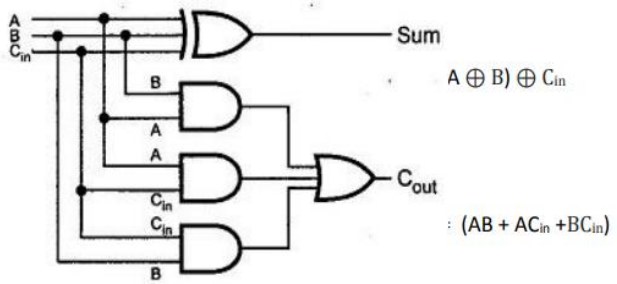
For Sum

A \ BC_{in}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$Sum = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

Logic Diagram:

(Note: Logic Diagram using basic or universal gate also can be consider)



7. Realize the basic logic gates, NOT, OR and AND gates using NOR gates only. 4M

Ans: **(NOT GATE USING NOR GATE:1 M)**

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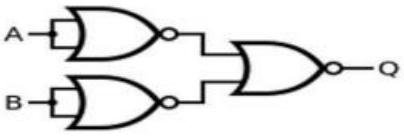
where, X = A NOR A

$x = \bar{A}$

(AND GATE USING NOR GATE:1.5 MARKS)

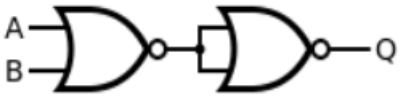


$\overline{Q}=\bar{A}+\bar{B} = \bar{A}+\bar{B}$

$=\overline{A.B}$

= A.B

(OR GATE USING NOR GATE:1.5 MARKS)



$Q=\overline{\overline{A+B}}$

=A+B

8. Describe the working of JK flip-flop with its truth table and logic diagram.

Ans: **(Diagram-2 M, Working-1M, Truth table-1M)**

Truth Table:

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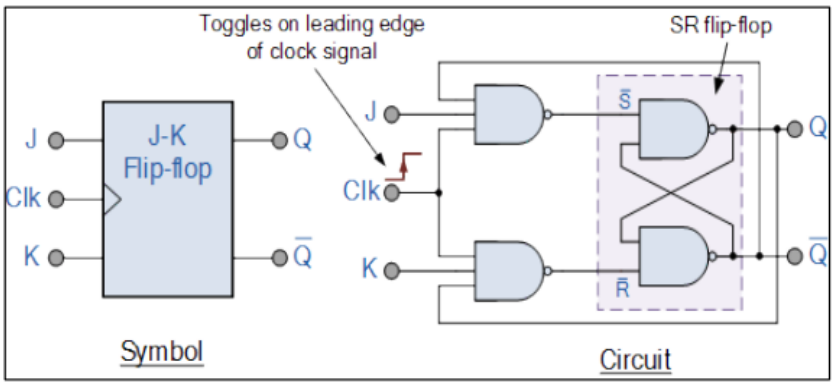
Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

Diagram:



Working:

The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”. Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”. Both the S and the R inputs of the previous SR bistable have now been replaced by two inputs called the J and K inputs, respectively after its inventor Jack Kilby. Then this equates to: J = S and K = R. The two 2-input AND gates of the gated SR bistable have now been replaced by two 3-input

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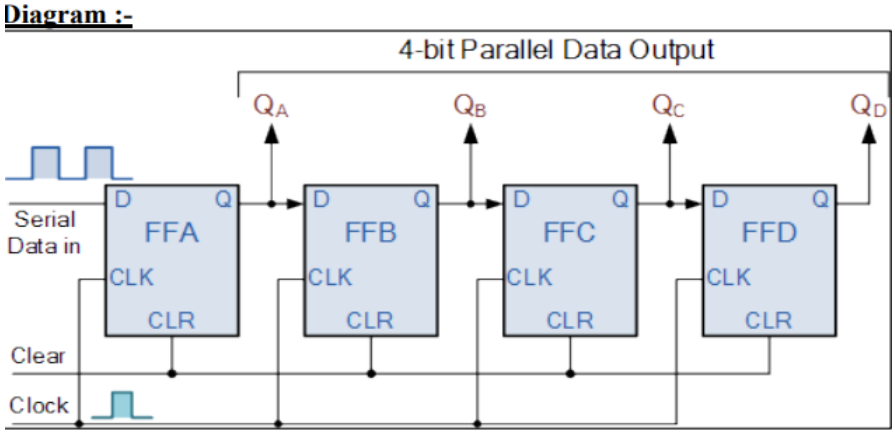
NAND gates with the third input of each gate connected to the outputs at Q and Q. This cross coupling of the SR flip-flop allows the previously invalid condition of S = "1" and R = "1" state to be used to produce a "toggle action" as the two inputs are now interlocked. If the circuit is now "SET" the J input is inhibited by the "0" status of Q through the lower NAND gate. If the circuit is "RESET" the K input is inhibited by the "0" status of Q through the upper NAND gate. As Q and Q are always different, we can use them to control the input. When both inputs J and K are equal to logic "1", the JK flip flop toggles

9. Draw and explain working of 4-bit serial Input parallel Output shift register.

Ans: **(Diagram:2M, Explaination:2M)**

Diagram :-



Explanation :-

If a logic "1" is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting QA will be set HIGH to logic "1" with all the other outputs still remaining LOW at logic "0". Assume now that the DATA input pin of FFA has returned LOW again to logic "0" giving us one data pulse or 0-1-0. The second clock pulse will change the output of FFA to logic "0" and the output of FF Band QB HIGH to logic "1" as its input D has the logic "1" level on it from QA. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at QA. When the third clock pulse arrives this logic "1" value moves to the output of FFC (QC) and so on until the arrival

30

of the fifth clock pulse which sets all the outputs QA to QD back again to logic level “0” because the input to FFA has remained constant at logic level “0”. The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of QA to QD. Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic “1” through the register from left to right as follows.

Basic Data Movement Through A Shift Register

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

10. Draw 16:1 MUX tree using 4:1 MUX.

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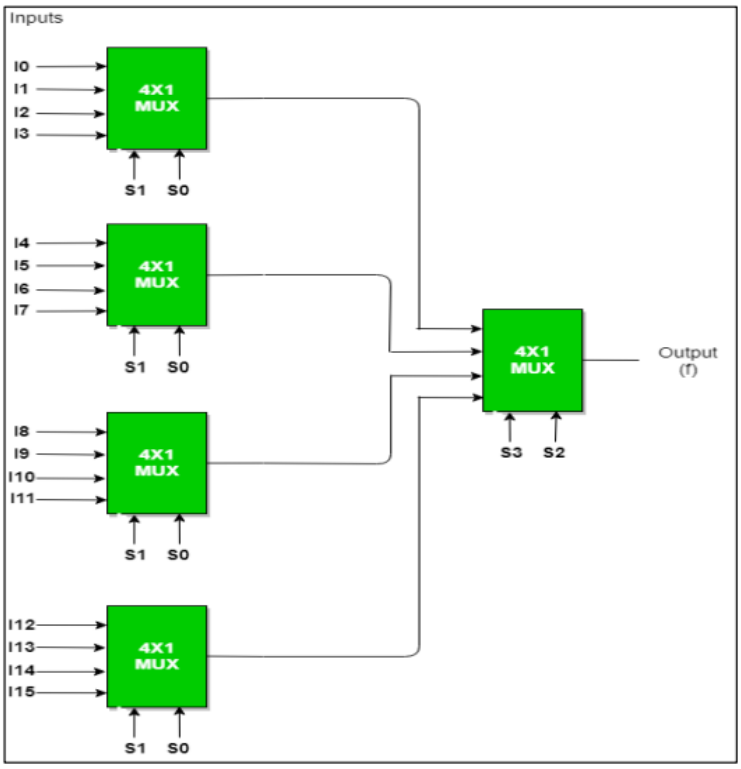
Ans: Diagram:



11. Calculate analog output of 4-bit DAC for digital input 1101. Assume VFS = 5V.

Ans: **(Formula- 1M, Correct problem solving- 3M)**

Formula :

VR = VFS

$$V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}]$$

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$= 5(1x2^{-1} + 1x2^{-2}+0x2^{-3}+1x2^{-4})$
$= 5(0.5+O.25+0+0.0625)$
$= 4.0625$ Volts

OR

$V_{FS} = V_R . (\frac{b3}{2} + \frac{b2}{4} + \frac{b1}{8} + \frac{b0}{16})$

Note – (Since V_R is not given find V_R)

Full Scale o/p mean

b3 b2 b1 b0 = 1111

$V_{FS} = 5V$

$5 = V_R . (\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16})$

$V_R = 5.33$

For digital i/p b3 b2 b1 b0 = 1101

$V_0 = 5.33 (\frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{1}{16})$

$V_0 = 4.33V$

12. State De Morgan's theorem and prove any one.

Ans: **(Each State and proof using table- 2M each)**

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i) $\overline{AB} = \overline{A} + \overline{B}$

It states that compliment of product is equal to sum of their compliments.

1	2	3	4	5	6
A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Column 03 = column 06

i.e. $\overline{AB} = \overline{A} + \overline{B}$

Hence proved

OR

ii) $\overline{A+B} = \overline{A} \cdot \overline{B}$

It states that complement of sum is equal to product of their complements.

1	2	3	4	5	6
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

Column 03 = column 06

$\therefore \overline{A+B} = \overline{A} \cdot \overline{B}$

Hence proved.

13. Design one digit BCD Adder using IC 7483

Ans: **(Diagram:4M)**

(Note: Labelled combinational circuit can be drawn using universal gate also)

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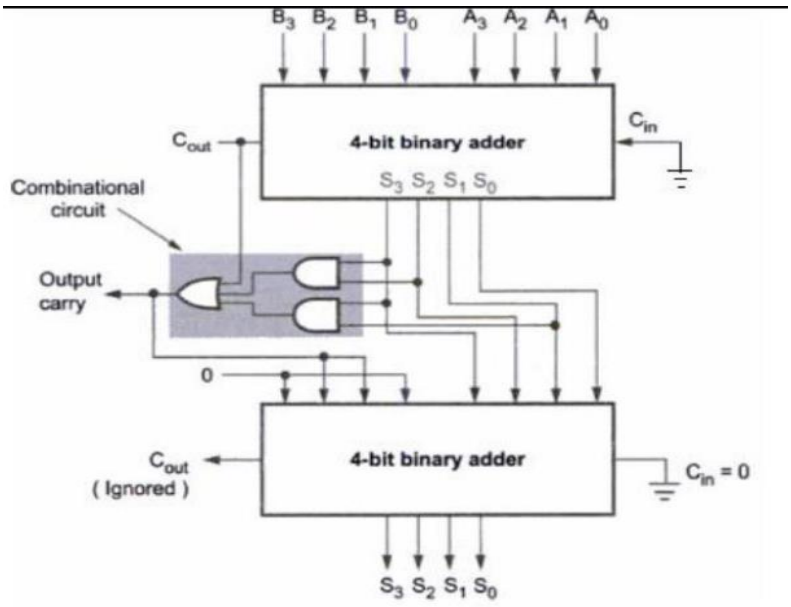

(SUMMER-19)

1. **Convert:**

(i) $(AD92.BCA)_{16} = (?)_{10} = (?)_8 = (?)_2$

Ans: **$(AD92.BCA)_{16}$**

$= (10 \times 16^3) + (13 \times 16^2) + (9 \times 16^1) + (2 \times 16^0) + (11 \times 16^{-1}) + (12 \times 16^{-2}) + (10 \times 16^{-3})$

$= 40960 + 3328 + 144 + 2 + 0.6857 + 0.046875 + 0.00244$

$= (44434.7368)_{10}$

OR **$(AD92.BCA)_{16} = (1010\ 1101\ 1001\ 0010.1011\ 1100\ 1010)_2$**

$(AD92.BCA)_{16} = (1010\ 1101\ 1001\ 0010.1011\ 1100\ 1010)_2$

$= (001\ 010\ 110\ 110\ 010\ 010.101\ 111\ 001\ 010)_2$

$= (126622.5712)_8$

Note: any other method can be considered.

2. Simplify the following and realize it

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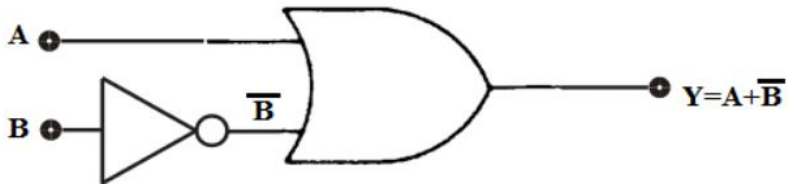
$Y = A + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C} + ABC + \overline{A}\overline{B}$

Ans:

$Y = A + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C} + ABC + \overline{A}\overline{B}$

$$Y = A + \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}\,\overline{C} + ABC + \overline{A}\,\overline{B}$$
$$= A(1 + BC) + \overline{A}\,\overline{B}(C + \overline{C}) + \overline{A}\,\overline{B}$$
$$= A + \overline{A}\,\overline{B} + \overline{A}\,\overline{B}$$
$$= A + \overline{A}\,\overline{B}$$
$$= (A + \overline{A}) \cdot (A + \overline{B})$$
$$= (A + \overline{B})$$



3. Explain the following characteristics w.r.t. logic families:

(i) Noise margin

(ii) Power dissipation

(iii) Figure of merit

(iv) Speed of operation

Ans: Noise margin: Noise margin indicates the amount to noise voltage circuit can tolerate at its input for both logic 1 and logic0.

Power Dissipation: It is the amount of power dissipated in an IC.

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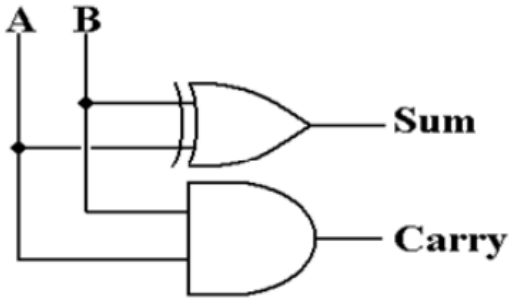
Figure of Merit: It is defined as the product of propagation delay and power dissipated by the gate.

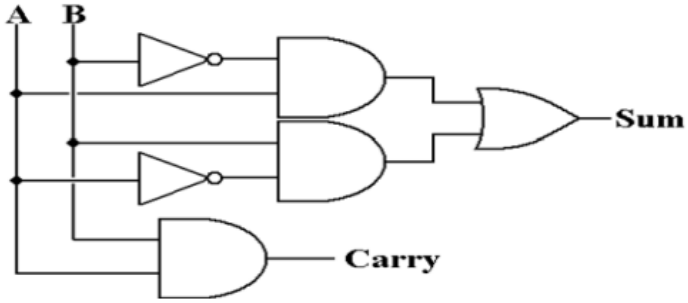
Speed of Operation: Speed of a logic circuit is determined by the time between the application of input and change in the output of the circuit.

4. Draw logic diagram of half adder circuit

Ans:



OR



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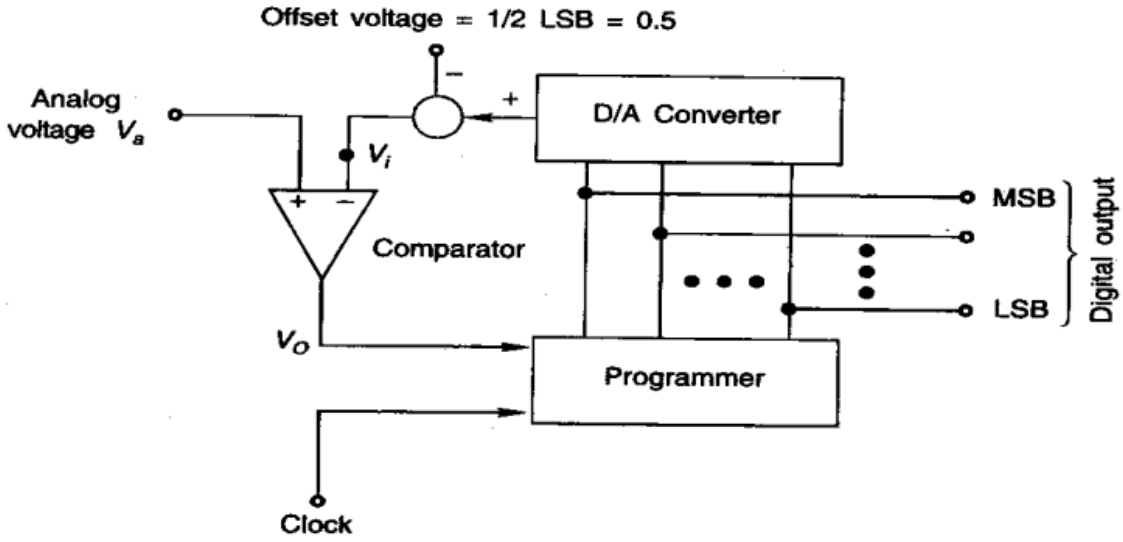
5. Draw the circuit of successive approximation type ADC and explain its working

Ans:



The successive approximation A/D converter is as shown in fig. An analog voltage (Va) is constantly compared with voltage Vi, using a comparator. The output produced by comparator (Vo) is applied to an electronic Programmer. If Va=Vi, then Vo=0 & then no conversion is required. The programmer displays the value of Vi in the form of digital O/P. But if Va Vi, then the O/P is changed by the programmer. If Va> Vi, then value of Vi is increased by 50% of earlier value. But if Va< Vi, then value of Vi is decreased by 50% of earlier value. This new value is converted into analog form, by D/A converter so as to compare it with Va again. This procedure is repeated till we get Va=Vi. As the value of Vi is changed successively, this method is called as successive-approximation A/D converter.

6. Describe the operation of R-S flip flop using NAND gates only.

Ans:

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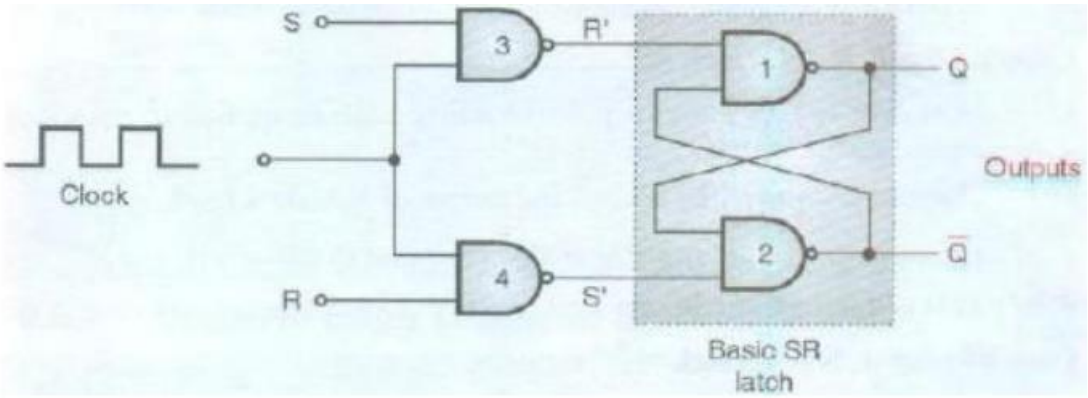

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Description/explanation-

When clock = 0, the outputs of NAND gates 3 and 4 will be forced to be 1 irrespective of the values of S and R. That means R'= S' = 1.Hence the outputs of basic SR/F/F i.e. Q n+1 and $\overline{Qn+1}$ will not change. Thus if clock = 0, then there is no change in the output of the clocked SR flip-flop.

Case I : S = R = 0, clock = 1: No change

If S=R=0 then outputs of NAND gate 3 and 4 are forced to become 1.
Hence R' and S' both will be equal to 1. Since R' and S' are the inputs of the basic S – R flip-flop using NAND gates. There will be no change in the state of outputs.

Case II : S =1, R = 0, clock = 1: Set

Now S=0, R=1 and a positive going edge is applied to the clock
Output of NAND 3 i.e. R' = 0 and output of NAND 4 i.e. S' = 1.
Hence output of SR flip-flop is Q n+1 = 1 and $\overline{Qn+1}$= 0.
This is the set condition.

Case III : S =0, R = 1, clock = 1: Reset

Now S=0, R=1 and a positive edge is applied to the clock input.
Since S=0, output of NAND – 3 i.e. R´= 1. And as R' = 1 and clock = 1 the output of NAND-4 i.e. S´ = 0. Hence output of SR flip-flop is Q n+1 = 0 and $\overline{Qn+1}$= 1.
This is the reset condition.

Case IV : S =1, R = 1, clock = 1: Undefined/ forbidden

As S=1, R=1 and clock = 1, the outputs of NAND gates 3 and 4 both are 0 i.e. S' = R'=0. So

CLK	INPUTS		OUTPUTS		REMARK
	S	R	Qn+1	$\overline{Qn+1}$	
0	X	X	Qn	$\overline{Qn}$	No change
1	0	0	Qn	$\overline{Qn}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	?	?	Forbidden

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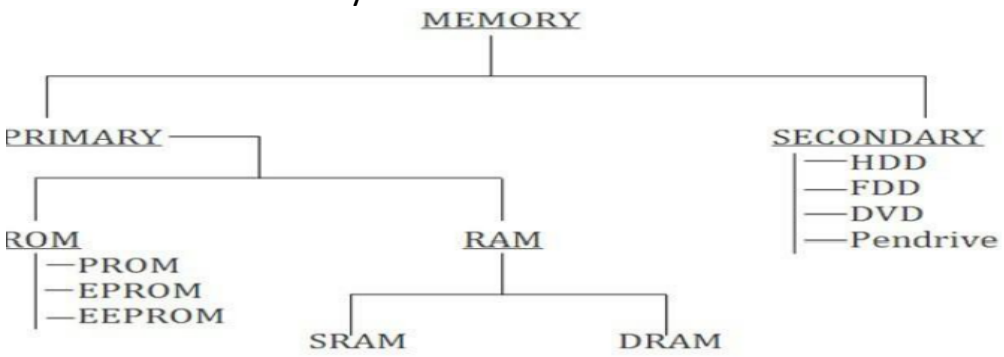
7. classification of memory and compare RAM and ROM **(any four points)**

Ans: classification of memory:



Comparison between RAM and ROM

RAM	RAM
1. Temporary Storage.	1.Permanent Storage.
2 .Store data in MBs.	2.Store data in GBs.
3. Volatile .	3.Non-Volatile
4. Writing data is Faster.	4.Writing data is Slower.

8. State the applications of shift register.

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Ans: 1] Shift register is used as Parallel to serial converter, which converts the parallel data into serial data. It is utilized at the transmitter section after Analog to Digital Converter (ADC) block.

2] Shift register is used as Serial to parallel converter, which converts the serial data into parallel data. It is utilized at the receiver section before Digital to Analog Converter (DAC) block.

3] Shift register along with some additional gate(s) generate the sequence of zeros and ones. Hence, it is used as sequence generator.

4] Shift registers are also used as counters. There are two types of counters based on the type of output from right most D flip-flop is connected to the serial input. Those are Ring counter and Johnson Ring counter.

9. Subtract the given number using 2's compliment method.

(i) $(11011)_2 - (11100)_2$

(ii) $(1010)_2 - (101)_2$

Ans:

i) **Subtract $(11011)_2 - (11100)_2$ using 2's complement binary arithmetic.**

Solution:

$(11011)_2 - (11100)_2$

Now,

2's complement of $(11100)_2$ = 1's complement of $(11100)_2$+1

1's complement of $(11100)_2$ = $(00011)_2$

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2's complement = 00011+1 = 00100

Therefore,

$$\begin{array}{r} 1\ 1\ 0\ 1\ 1 \\ + \\ 0\ 0\ 1\ 0\ 0 \\ \hline 1\ 1\ 1\ 1\ 1 \end{array}$$

There is no carry it indicates that results is negative and in 2's complement form i.e.$(11111)_2$.

Therefore, for getting true value i.e.(+1) take 2's complement of (11111) is

1's complement + 1

= 00000 + 1

Ans= $(00001)_2$

Ans: $(11011)_2 - (11100)_2$ = 2's complement of $(11111)_2 = (-1)_{10}$

ii) Subtract $(1010)_2$ - $(101)_2$using 2's complement binary arithmetic.

2's complement of $(0101)_2$ = 1's complement of $(0101)_2$ +1

1's complement of $(0101)_2$ = $(1010)_2$

2's complement = 1010+1 = 1011

Therefore,

$$\begin{array}{r} 1\ 0\ 1\ 0 \\ + \\ 1\ 0\ 1\ 1 \\ \hline 1\ 0\ 1\ 0\ 1 \end{array}$$

(1 is the carry)

There is carry ignore it, which indicates that results is positive i.e.(+5)

= $(0101)_2$

Ans: $(1010)_2$ - $(101)_2$ = $(0101)_2 = (+5)_{10}$

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10. State De-Morgan's theorem and prove any one.

Ans: De Morgan´s 1st Theorem: It states that the compliment of sum is equal to the product of the compliment of individual variables.

$$\overline{(A + B)} = \overline{A}\ \overline{B}$$

Proof:

A	B	$\overline{A}$	$\overline{B}$	A+B	$\overline{(A + B)}$		$\overline{A}\ \overline{B}$
0	0	1	1	0	1		1
0	1	1	0	1	0		0
1	0	0	1	1	0		0
1	1	0	0	1	0		0

De Morgan´s 2nd Theorem: It states that the compliment of product is equal to the sum of the compliments of individual variables.

$$\overline{(A\,B)} = \overline{A} + \overline{B}$$

Proof:

A	B	$\overline{A}$	$\overline{B}$	A.B	$\overline{(A\,B)}$	$\overline{A} + \overline{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

11. Compare between PLA and PAL.

Ans:

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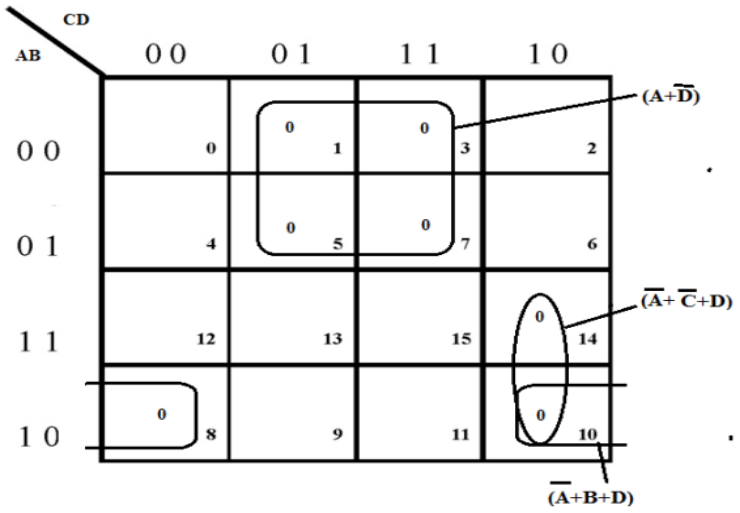
PLA	PAL
1) Both AND and OR arrays are programmable	1) OR array is fixed and AND array is programmable.
2) Costliest and complex than PAL	2) Cheaper and simpler
3) AND array can be programmed to get desired minterms.	3) AND array can be programmed to get desired minterm.
4) Large number of functions can be implemented.	4) Provides the limited number of functions.
5) Provides more programming flexibility.	5) Offers less flexibility, but more likely used.

12. Reduce the following expression using K-map and implement it.

F(A,B,C,D) = M (1,3,5,7,8,10,14)

Ans:



F(A,B,C,D)=(A+$\overline{D}$) ($\overline{A}$+$\overline{C}$+D) ($\overline{A}$+B+D)

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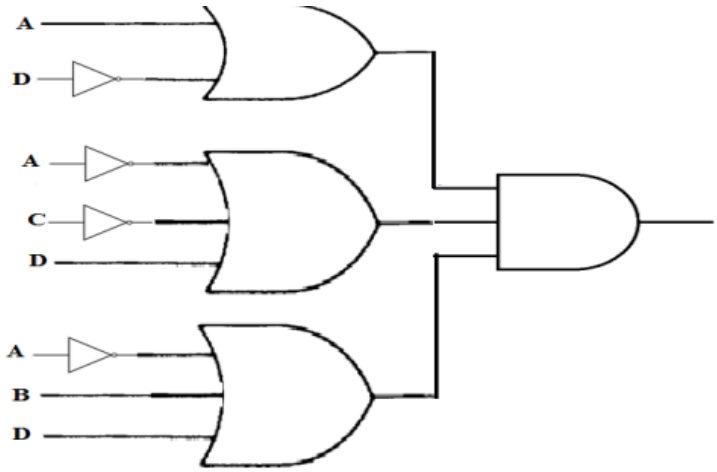
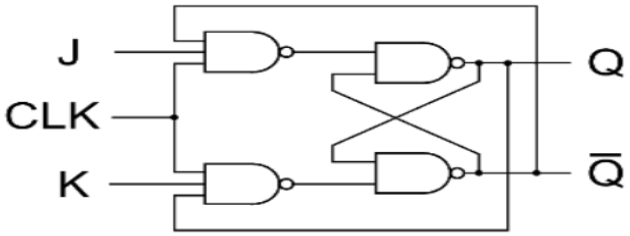


12. Describe the working of J-K flip-flop and state the race around condition.

Ans:



Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

The clock signal is applied to CLK input.

IF CLK =0 than F/F is disabled and O/P Q and $\bar{Q}$ do not change

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If CLK= 1 and J=K=O then the output Q and $\bar{Q}$ will not change their state.

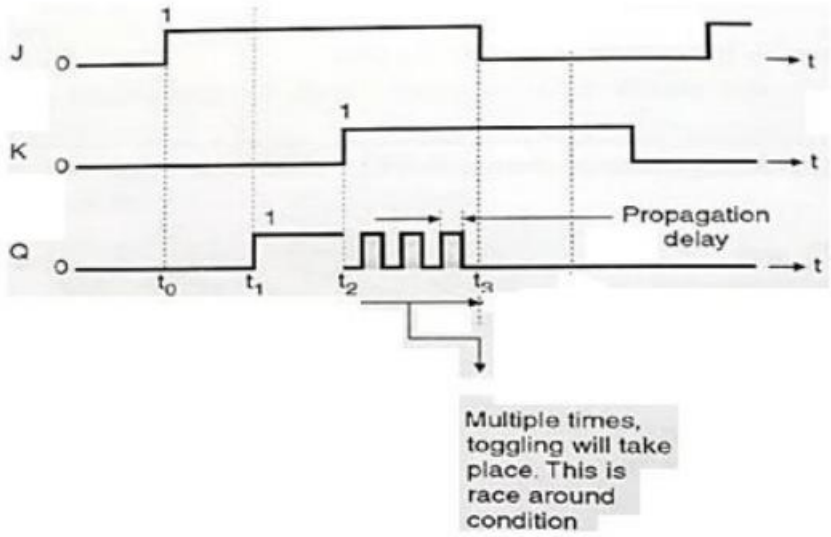
If J=0 and K= 1 then JK flip flop will reset and Q= 0 & $\bar{Q}$ =1

If J=1 and K=0 then output will be set and Q=1 & $\bar{Q}$ =0

If J= K=1 then Q & $\bar{Q}$ outputs are inverted and FF will toggle

Race Around condition:

Race around condition occurs in J K Flip-flop only when J=K=1 and clock/enable is high (logic 1) as shown below-



In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state), but due to multiple feedback, output changes/toggles many times till the clock/enable is high.

Thus toggling takes place more than once, called as racing or race around condition.

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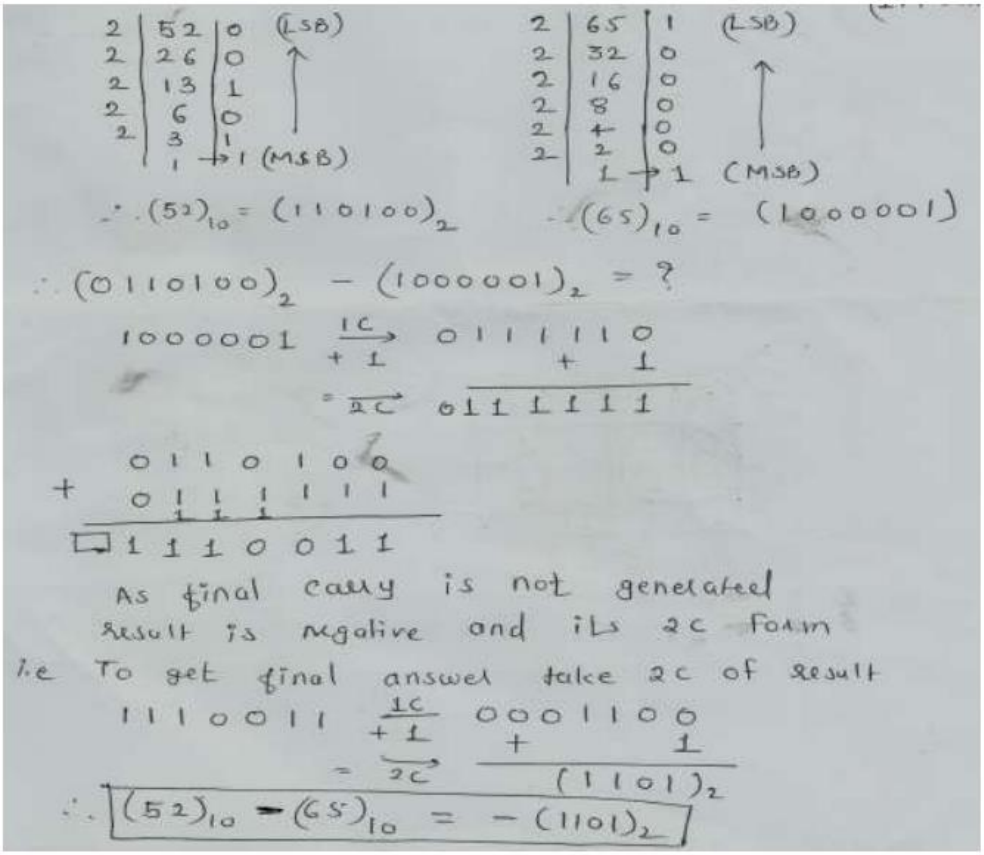
(WINTER-19)

1. Perform the subtraction using 2'S Complement methods.

$(52)_{10} - (65)_{10}$

Ans:

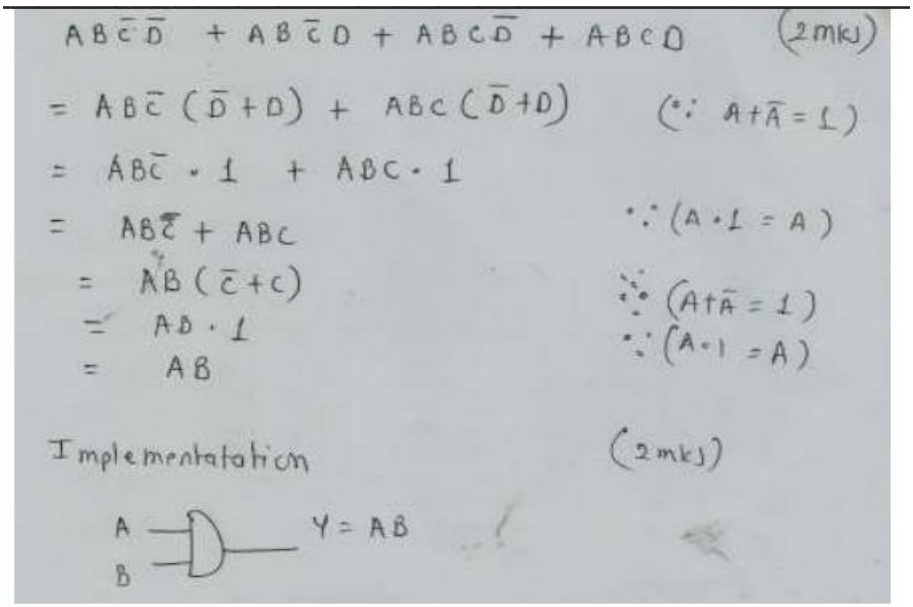


2. Simplify the following Boolean Expression and Implement using logic gate.

$AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD$

Ans:

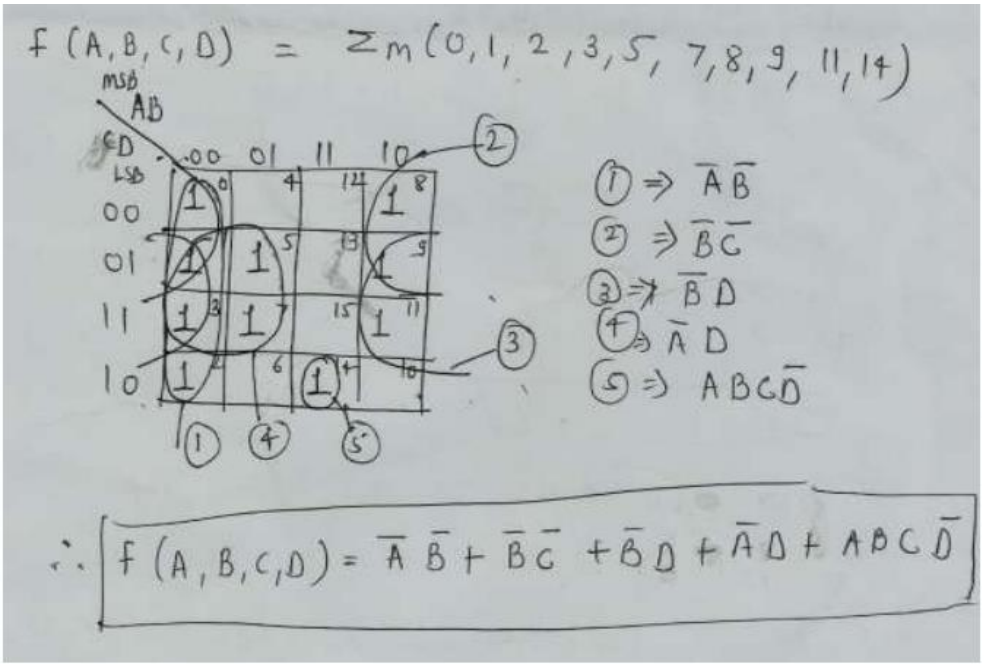
48



3. Minimize the four variable logic function using K map.

F(A,B,C,D) = ∑m(0,1,2,3,5,7,8,9,11,14)

Ans:



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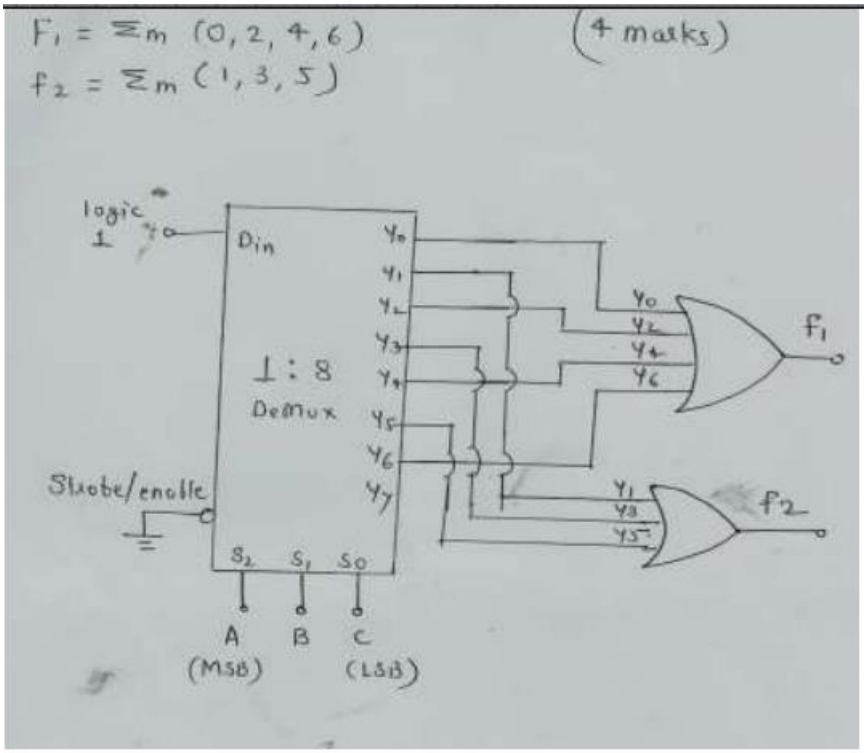
4. Implement the following function using demultiplexer.

f1 = ∑m(0,2,4,6)

f2 = ∑m(1,3,5)

Ans:



5. Realize the following logic expression using only NAND gates.

(i) OR

(ii) AND

(iii)NOT

Ans:

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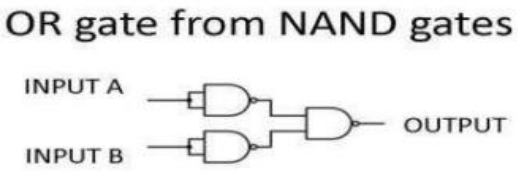
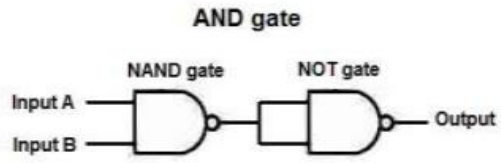
(i)OR



(ii)AND



(ii)NOT

6. Draw binary to Gray converter and write its truth table.

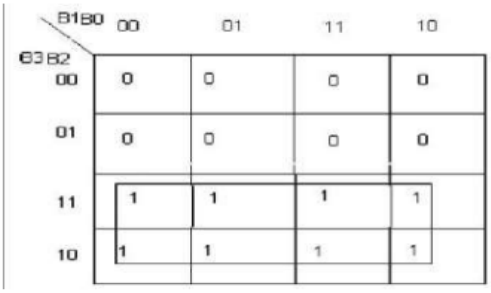
Ans:

51

Truth Table for 4 bit Binary to Gray code converter

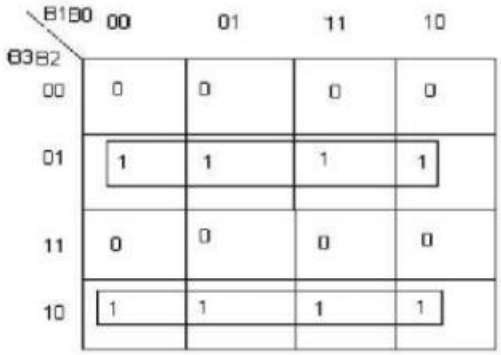
Binary Input				Gray Output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

K-MAP FOR G3:



G3=B3

K-MAP FOR G2



$G2 = \overline{B3}B2 + \overline{B2}B3$

=B3 XOR B2

K-MAP FOR G1:

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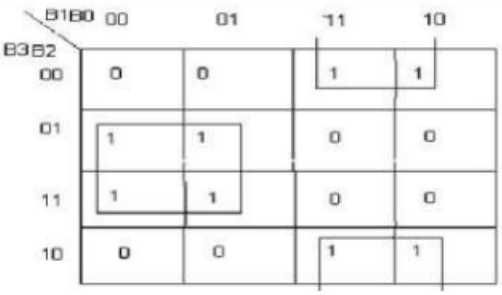
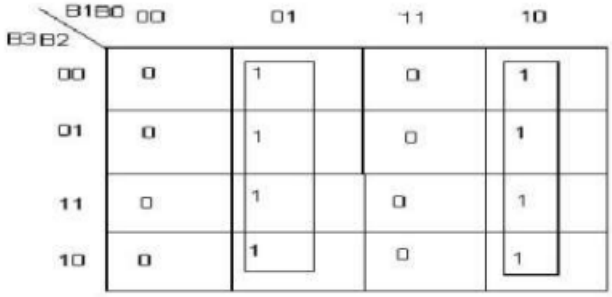


$G1=\overline{B2}\,B1 + B2\,\overline{B1}$

= B1 XOR B2

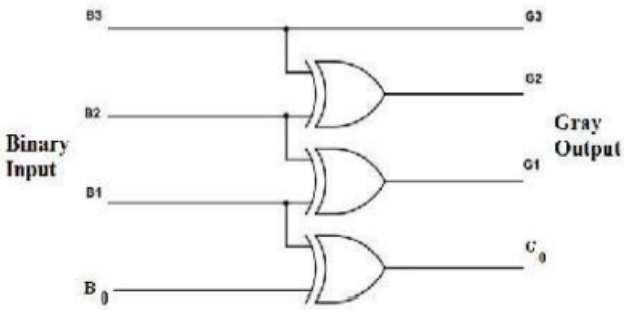
K-MAP FOR G0:



$G0 = \overline{B1}B0 + B1\overline{B0}$

= B1 XOR BO

Diagram for 4 bit Binary to Gray code converter:



(Note: Realization of output equation can be done Basic or Universal)

7. Describe the working of JK flip flop with truth table and logic Diagram.

Ans: Logic Diagram:

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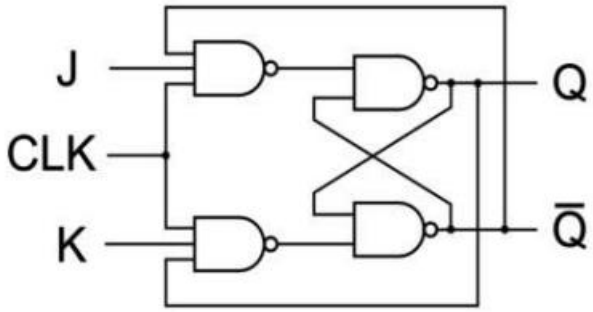

Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

Working:

The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”. Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”. Both the S and the R inputs of the previous SR bistable have now been replaced by two inputs called the J and K inputs, respectively after its inventor Jack Kilby. Then this equates to: J = S and K = R. The two 2-input AND gates of the gated SR bistable have now been replaced by two 3- input NAND gates with the third input of each gate connected to the outputs at Q and Q. This cross coupling of the SR flip-flop allows the previously invalid condition of S = “1” and R = “1” state to be used to produce a “toggle action” as the two inputs are now interlocked. If the circuit is now “SET” the J input is inhibited by the “0” status Of Q through the lower NAND gate. If the circuit is “RESET” the K input is inhibited by the “0” status of Q through

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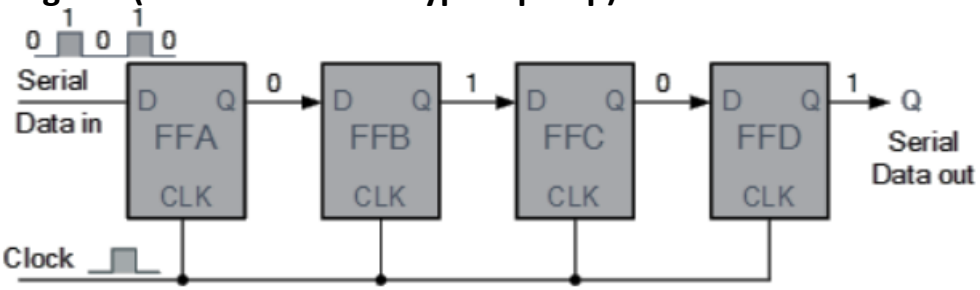
the upper NAND gate. As Q and Q are always different, we can use them to control the input. When both inputs J and K are equal to logic “1”, the JK flip flop toggles.

8. Describe the working of 4 bit SISO (serial in serial out) shift register with diagram and waveform if input is 01101.

Ans: **Diagram:(use SR or JK or D type flip flop)**



Working:

The DATA leaves the shift register one bit at a time in a serial pattern, hence the name Serial-in to Serial-Out Shift Register or SISO. The SISO shift register is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left-hand flip-flop, the serial output (SO) which is taken from the output of the right-hand flip-flop and the sequencing clock signal (Clk). The logic circuit diagram below shows a generalized serial in serial-out shift register, Output of FFA is Q4, FFB Q3, FFC Q2 and FFD is Q1

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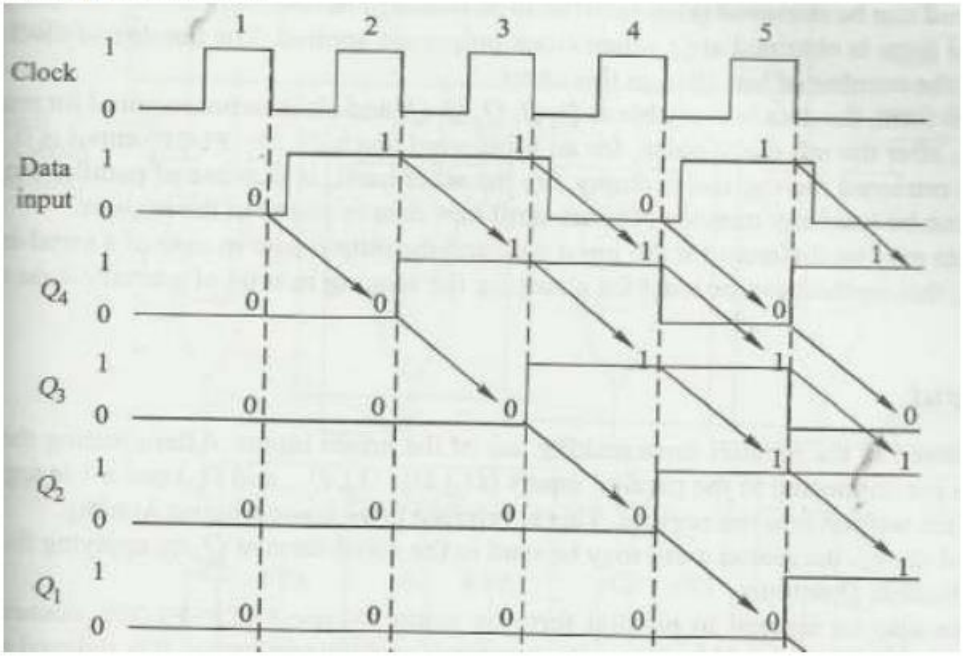
Waveform:(Input is 01101)



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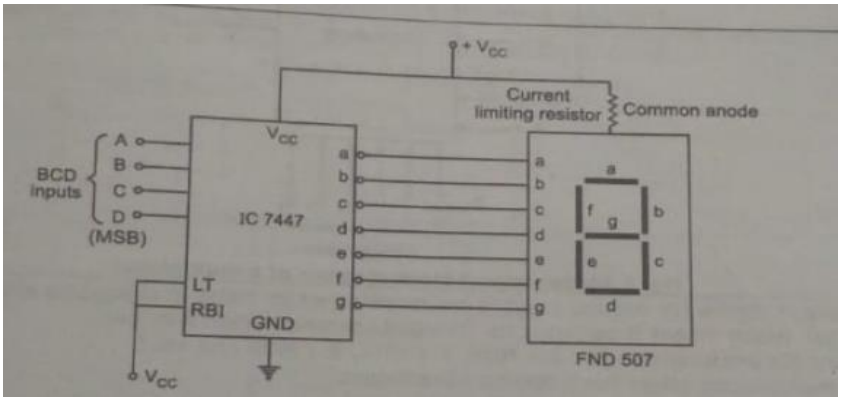
(SUMMER-22)

2. Draw circuit diagram of BCD to seven segment decoder and write its truth table.

Ans:



Decimal digit	8-4-2-1 BCD inputs				Output in seven segment code						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	0	1	0	1	1	0	0	0	0
0	0	0	1	0	1	1	0	1	1	0	1
0	0	0	1	1	1	1	1	1	0	0	1
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	0	1	1	0	1	1	0	1	1
0	0	1	1	0	1	0	1	1	1	1	1
0	0	1	1	1	1	1	1	0	0	0	0
0	1	0	0	0	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1

3. Draw the block diagram of programmable array logic.

Ans:

57

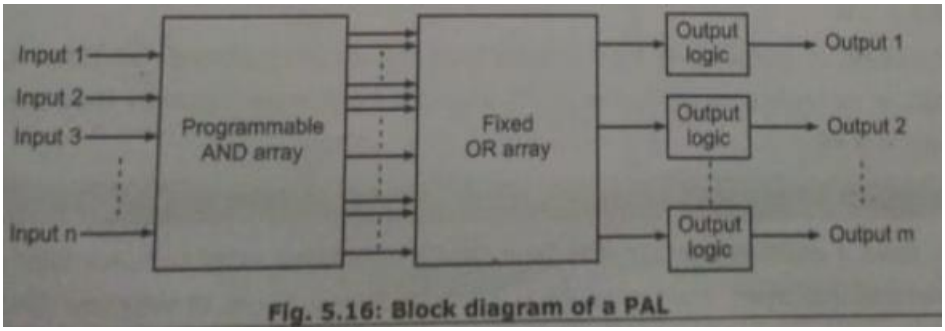
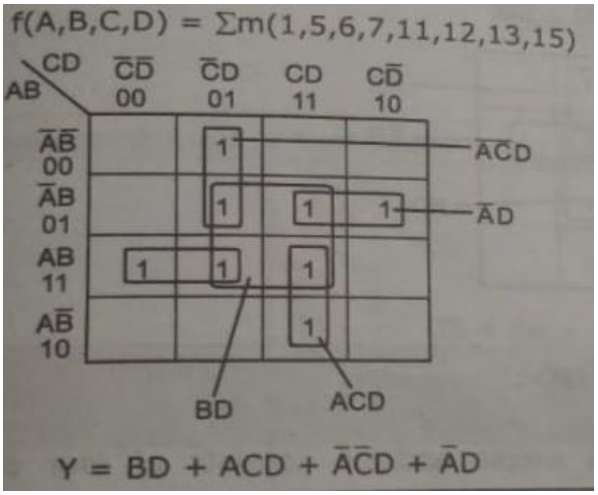


Fig. 5.16: Block diagram of a PAL

4. Minimize following expression using K-map. f(A,B,C,D) = Σm (1,5,6,7,11,12,13,15)

Ans:



5. Realize the following logic operation using only NOR gates:
AND, OR, NOT.

Ans:

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1. NOT Gate using NOR Gate:

Expression for NOR gate is $Y = \overline{A + B}$

Expression for NOT gate is $Y = \overline{A}$

If we short both the inputs of NOR gate, then A = B.

$\therefore \quad Y = \overline{A + A} = \overline{A}$ = Expression for NOT gate ($\because A + A = A$)

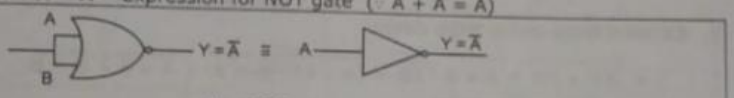


Fig. 2.20

2. AND Gate using NOR Gate: S-10; W-12, 11

- Expression for AND gate is $Y = AB = \overline{\overline{AB}}$ ($\because \overline{\overline{A}} = A$)

Applying De Morgan's second theorem, $Y = \overline{\overline{A} + \overline{B}}$, we can implement using NOR gates at this stage.

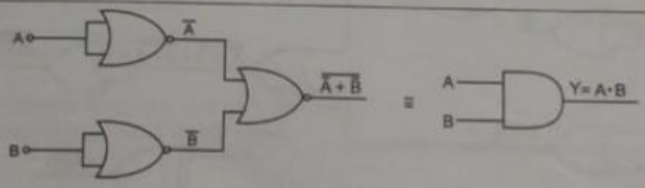


Fig. 2.21

OR Gate using NOR Gate: W-14

Expression for OR gate is $Y = A + B = \overline{\overline{A + B}}$

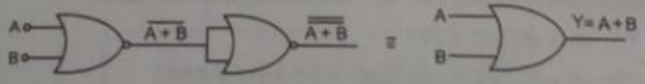
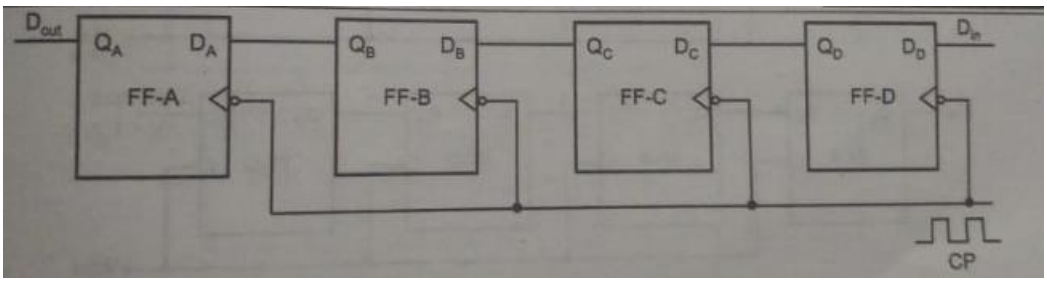


Fig. 2.22

6. Describe the operation of 4 bit serial in serial out shift register

Ans:



Working:

The operation of a SISO shift register relies on two primary components: the flip-flops and the clock signal.

1. **Flip-Flops**: A flip-flop is a fundamental building block of sequential circuits. In the case of a SISO shift register, each flip-flop stores a single bit of data. The number of flip-flops determines the length or size of the shift register.

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2. **Clock Signal**: The clock signal synchronizes the movement of data through the shift register. With each clock pulse, the data shifts from one flip-flop to the next. The clock signal ensures that the data propagates in a controlled and synchronized manner.

When the clock signal transitions from low to high (or high to low, depending on the specific implementation), the input data is sampled and stored in the first flip-flop. On subsequent clock pulses, the stored data moves through the chain of flip-flops. The output of the shift register is taken from the last flip-flop in the series.

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6 MARKS QUESTIONS
(WINTER-18)

1. Subtract using 2's compliment method

$(35)_{10} - (5)_{10}$

Ans:

Step 1 – Obtain binary equivalent of $(35)_{10}$& $(5)_{10}$ & then take 2's compliment of $(5)_{10}$.

i.e. $(35)_{10} = (100011)_2$

$(5)_{10} = (101)_2$

2's compliment of $(5)_{10} = (000101)_2 =$ 111010 → 1's compliment

\+ 1

$(111011)_2$ → 2's Compliment

Step -2 :

Now add $(100011)_2$ and $(111011)_2$

100011

\+ 111011

---

1 | 011110

→ Carry is generated so answer is in positive form, so will discard the carry generated

Therefore final answer will be **$(011110)_2 = (30)_2$**

2. Design a 4-bit synchronous counter and draw its logic diagram.

Ans:

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State Table:

Present state				Next state				Flip flop inputs			
D	C	B	A	D^+	C^+	B^+	A^+	T_D	T_C	T_B	T_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0	1	1	1	1

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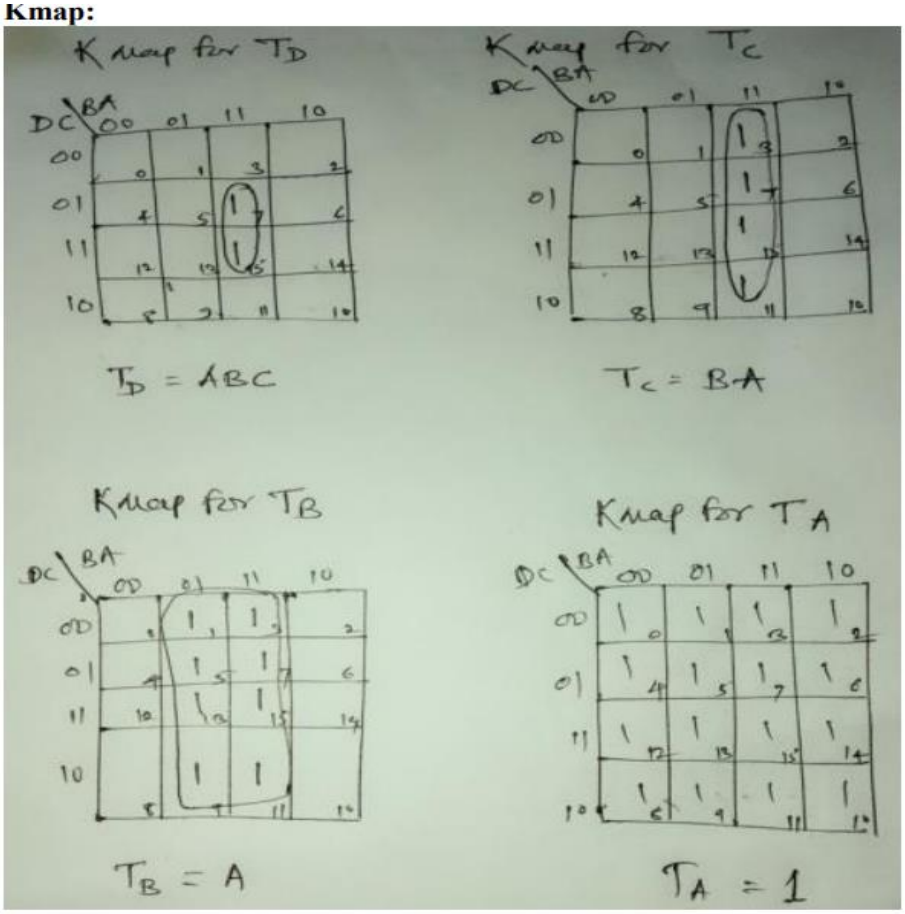
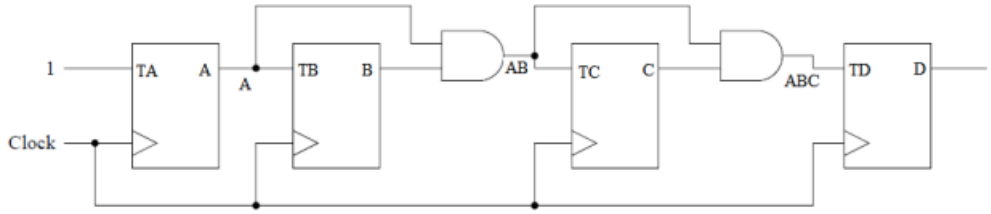
Kmap:



Logic Diagram:

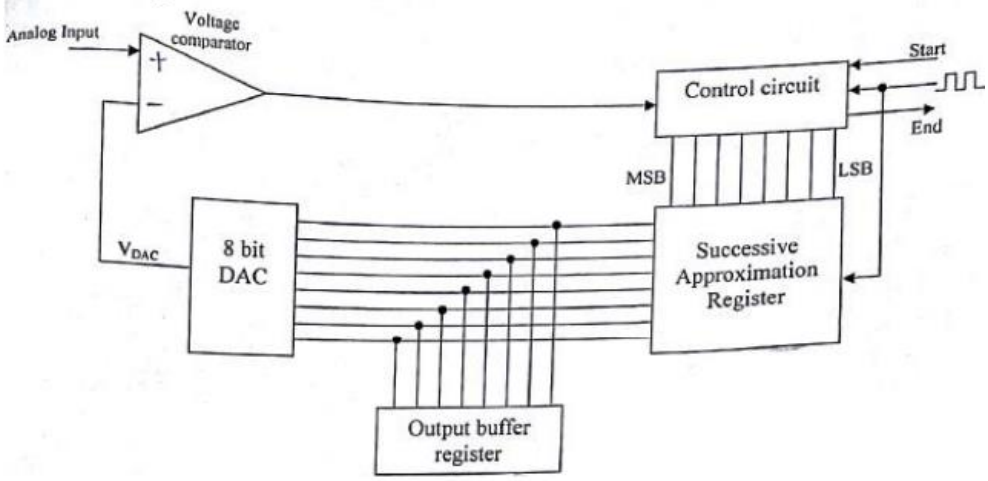


3. Describe the working of Successive Approximation ADC. Define Resolution and conversion time associate with ADC.

Ans:

63

Circuit Diagram:



When the start signal goes low the successive approximation register SAR is cleared and output voltage of DAC will be 0V. When start goes high the conversion starts.

After starts, during first clock pulse the control circuit set MSB bit so SAR output will be 1000 0000. This is connected as input to DAC so output of DAC is (analog output) compared with V_{in} input voltage. If V_{DAC} is more than V_{in} the comparator output $-V_{sat}$, if V_{DAC} is less than V_{in}, the comparator output is $+V_{sat}$.

If output of DAC i.e. V_{DAC} is $+ V_{sat}$ (i.e unknown analog input voltage $V_{in} > V_{DAC}$) then MSB bit is kept set, otherwise it is reset.

Consider MSB is set so SAR will contain 1000 0000.

The next clock pulse will set next bit i.e D_6 a digital output of 1100 0000. The output voltage of DAC i.e V_{DAC} is compared with V_{in}, if it is $+ V_{sat}$ the D_6 bit is kept as it is, but if it is $-V_{sat}$ the D_6 bit reset.

The process of checking and taking decision to keep bit set or to reset is continued upto D_0.

Then the DAC input will be digital data equal to analog input.

When the conversation if finished the control circuits sends out an end of conversion signal and data is locked in buffer register

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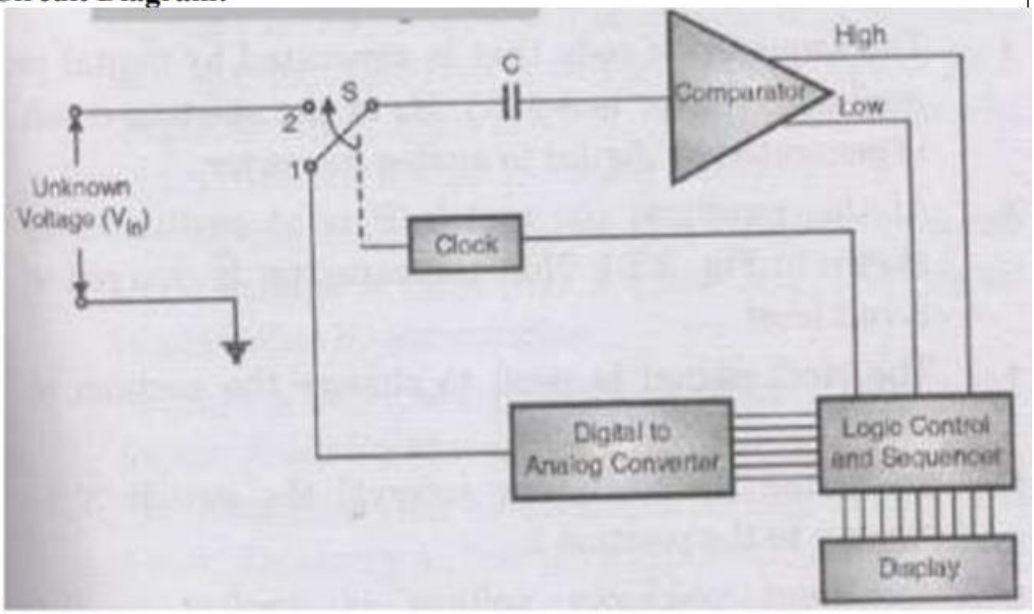
Resolution: The voltage input change necessary for a one bit change in the output is called resolution.

Conversion Time: The conversion time is the time required for conversion from an analog input voltage to the stable digital output

OR

Circuit Diagram:



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Explanation:

DAC= Digital to Analog converter
EOC= End of conversion
SAR =Succesive approximation register
S/H= Sample and hold circuit
Vin= input voltage
Vref= reference voltage
The successive approximation Analog to Digital converter circuit typically consisting of four sub circuits-
1. A sample and hold circuit to acquire the input voltage Vin.
2. An analog voltage comparator that compares Vin to the output of internal DAC and outputs the result of comparison to successive approximation register(SAR).
3. SAR sub circuits designed to supply an approximate digital code of Vin to the internal DAC.
4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of digital code output of SAR for comparison with Vin.

The successive approximation register is initialized so that most significant bit (MSB) is equal to digital 1. This code is fed into DAC which the supplies the analog equivalent of this digital code Vref/2 into the comparator circuit for the comparison with sampled input voltage. If this analog voltage exceeds Vin the comparator causes the SAR to reset the bit, otherwise a bit is left as 1. Then the

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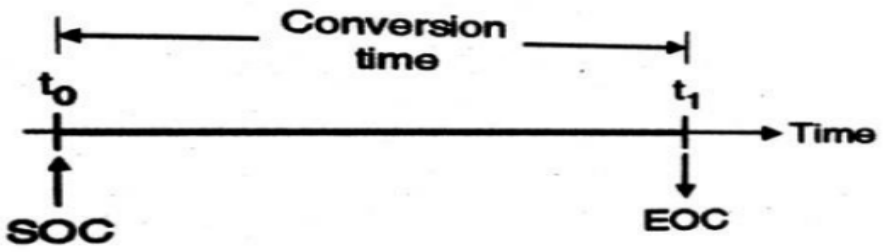
next bit is set to 1 and the same test is done continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by DAC at end of the conversion (EOC).

Resolution and conversion time associate with ADC-

Resolution:
It is the maximum number of digital output codes.
Resolution= 2^n
(OR)
It is defined as the ratio of change in the value of input analog voltage required to change the digital output by 1 LSB.

$$\therefore \text{ Resolution } = \frac{V_{FS}}{2^n - 1}$$

Conversion time:
The time difference between two instants i.e. 'to' where SOC signal is given as input to the ADC and 't1' where EOC signal we get as output from ADC. it should be small as possible.



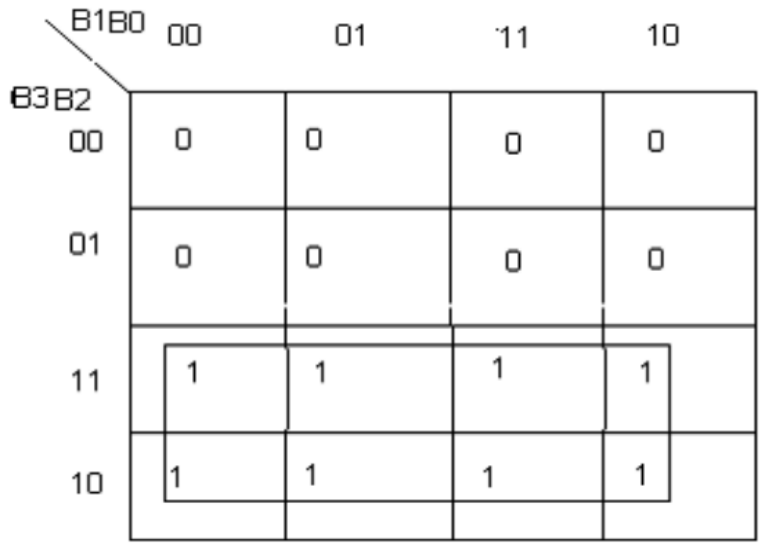
4. Design 4 bit Binary to Gray code converter
Ans:

67

Truth Table for 4 bit Binary to Gray code converter

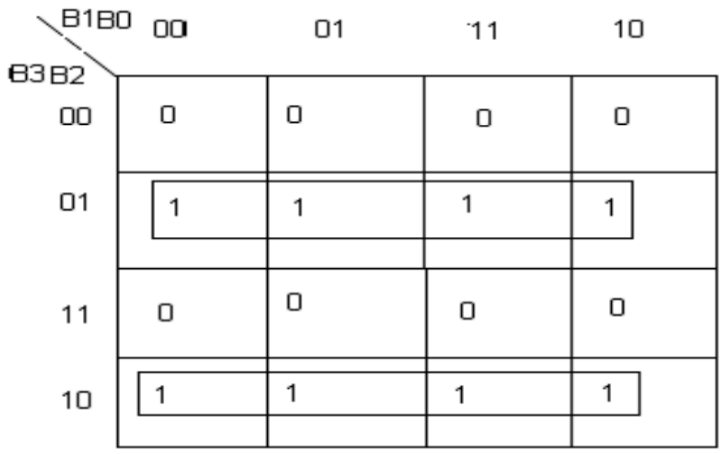
Binary Input				Gray output			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

K-MAP FOR G3:



G3=B3

68



K-MAP FOR G2:

$G2=\overline{B3}\ B2+\overline{B2}\ B3$

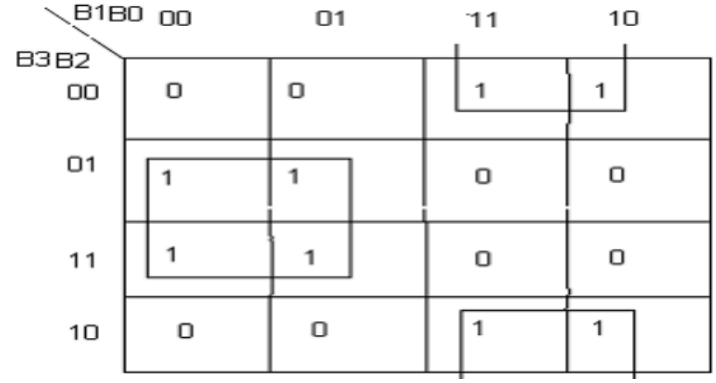
= B3 XOR B2

K-MAP FOR G2:

$G2=\overline{B3}\ B2+\overline{B2}\ B3$

= B3 XOR B2

K-MAP FOR G1:



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$G1=\overline{B2}\,B1 + B2\,\overline{B1}$

= B1 XOR B2

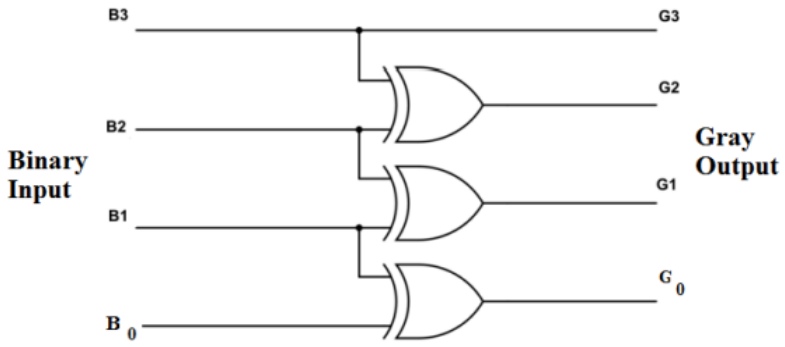
K-MAP FOR G0:

B3B2 \ B1B0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$G0=\overline{B1}B0 + B1\overline{B0}$

= B1 XOR B0

Diagram for 4 bit Binary to Gray code converter:



Note: Realization of output equations can be done using Basic or Universal gates

5. Compare the following (Any three points)

i) Volatile with Non-volatile memory

ii) SRAM with DRAM memory

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Ans:

Parameter	Volatile memory	Non-Volatile memory
definition	Memory required electrical power to keep information stored is called volatile memory	Memory that will keep storing its information without the need of electrical power is called nonvolatile memory.
classification	All RAMs	ROMs, EPROM, magnetic memories
Effect of power	Stored information is retained only as long as power is on.	No effect of power on stored information
applications	For temporary storage	For permanent storage of information

2. SRAM with DRAM memory

Parameter	SRAM	DRAM
Circuit configuration	Each SRAM cell is a flip flop	Each cell is one MOSFET & a capacitor
Bits stored	In the form of voltage	In the form of charges
No of components per cell	More	Less
Storage capacity	Less	More
Refreshing	It does not require refreshing	It require refreshing.
Cost	It is expensive	It is cheaper
Speed	It is faster	It is slower comparatively

6. Give block schematic of decade counter IC 7490. Design Mod-7 counter using this IC.
Ans:

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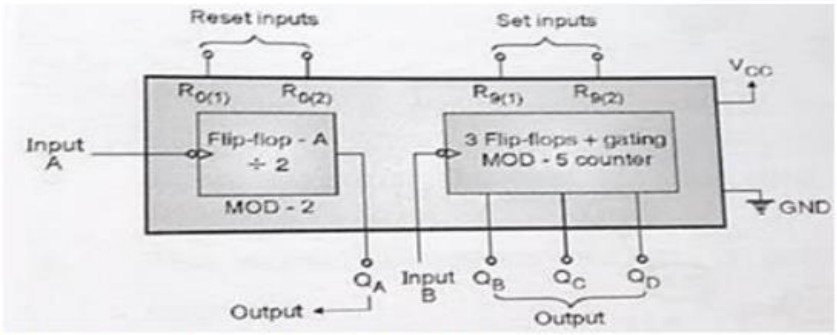
1. block schematic of decade counter IC 7490-



Mod-7 means states are from o,1,2,3,4,5,6,0
Therefore we have to reset counter IC 7490 when Q_D,Q_C,Q_B,Q_A=0111
Design reset logic:
Output of reset circuit should be HIGH because R0(1) and R0(2) are active high inputs.
Therefore reset logic output should be low for states 0 to 6.

Output should be HIGH for states 7 onwards.

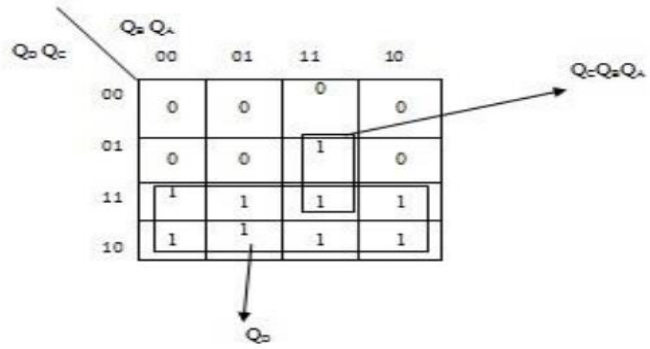
Truth table & K-map:

Q_D	Q_C	Q_B	Q_A	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1

Invalid State

For Y

72

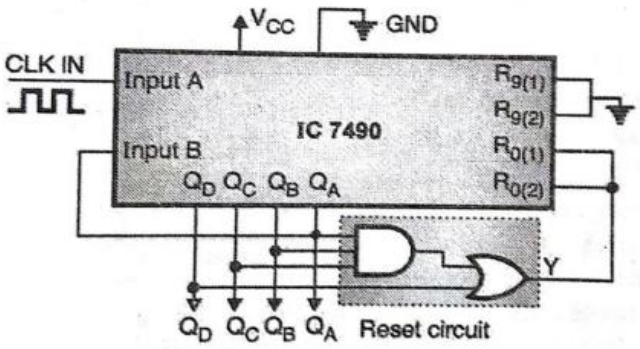


Expression for Y:

$$Y = Q_C\, Q_B\, Q_A + Q_D$$

Circuit is-

Logic Diagram:



(SUMMER-19)

1. Design BCD to seven segment decoder using IC 7447 with its truth table.

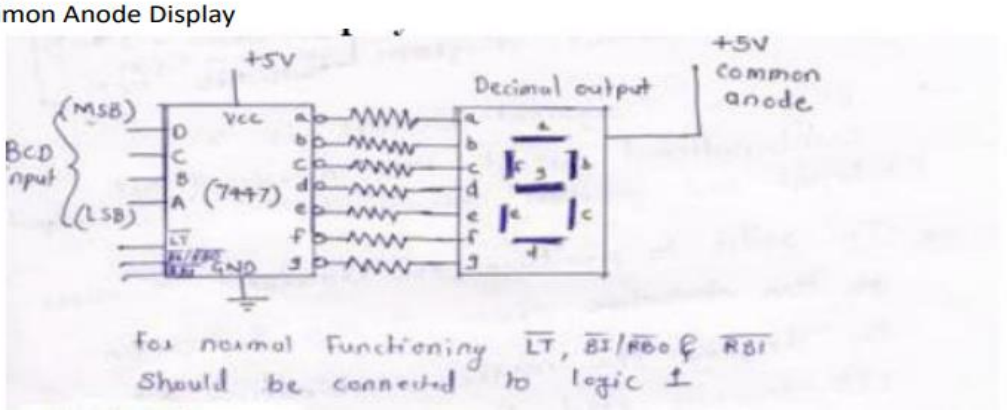
Ans:

73

Note: Any one type of display shall be considered

1. BCD to 7 segment decoder is a combinational circuit that accepts 4 bit BCD input and generates appropriate 7 segment output.
2. In order to produce the required numbers from 0 to 9 on the display the correct combination of LED segments need to be illuminated.
3. A standard 7 segment LED display generally has 8 input connections, one from each LED segment & one that acts as a common terminal or connection for all the internal segments
4. Therefore there are 2 types of display 1. Common Anode Display 2. Common Cathode Display :

Common Anode Display



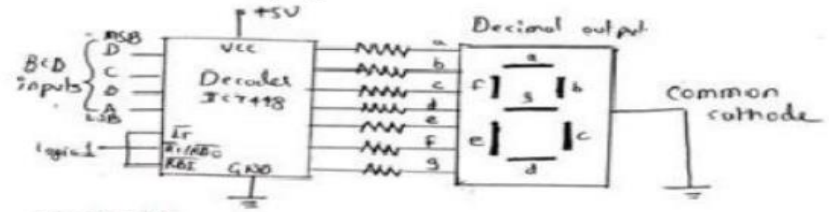
Truth Table

For Seven segment decoder using common anode display

BCD Inputs				7 segment coded outputs							Display outputs
D	C	B	A	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	1	1	0	0	1	1	1	1	
0	0	1	0	0	0	1	0	0	1	0	
0	0	1	1	0	0	0	0	1	1	0	
0	1	0	0	1	0	0	1	1	0	0	
0	1	0	1	0	1	0	0	1	0	0	
0	1	1	0	1	1	0	0	0	0	0	
0	1	1	1	0	0	0	1	1	1	1	
1	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	1	1	0	0	

74

Common Cathode Display:

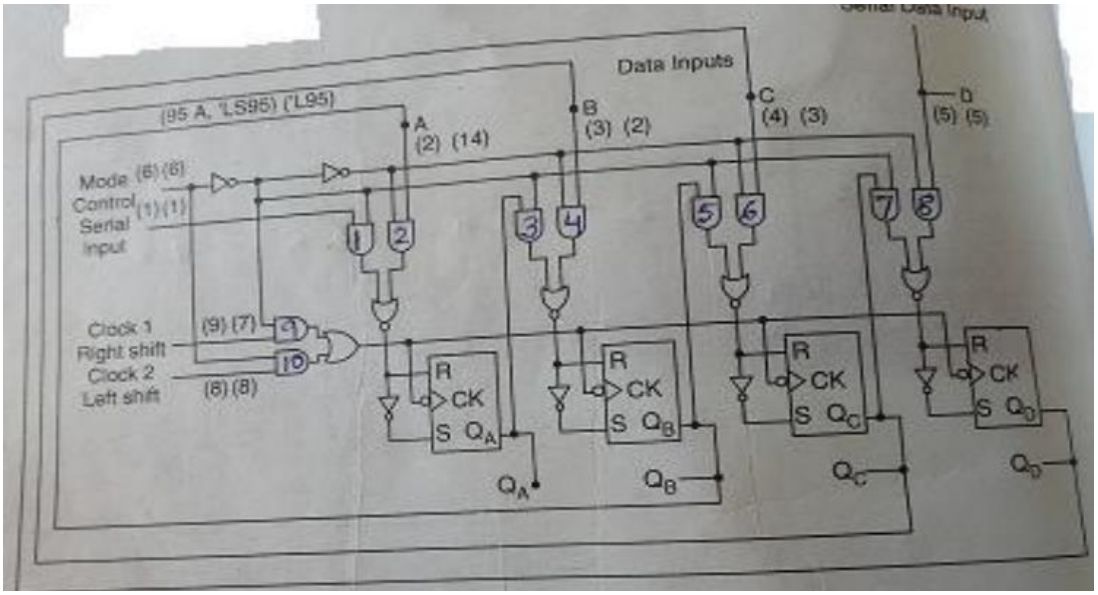


Truth Table

BCD inputs				7 segment coded outputs							Display output
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	
0	0	0	1	0	1	1	0	0	0	0	
0	0	1	0	1	1	0	1	1	0	1	
0	0	1	1	1	1	1	1	0	0	1	
0	1	0	0	0	1	1	0	0	1	1	
0	1	0	1	1	0	1	1	0	1	1	
0	1	1	0	0	0	1	1	1	1	1	
0	1	1	1	1	1	1	0	0	0	0	
1	0	0	0	1	1	1	1	1	1	1	
1	0	0	1	1	1	1	0	0	1	1	

2. Describe the working of 4-bit universal shift register.

Ans:



Working:

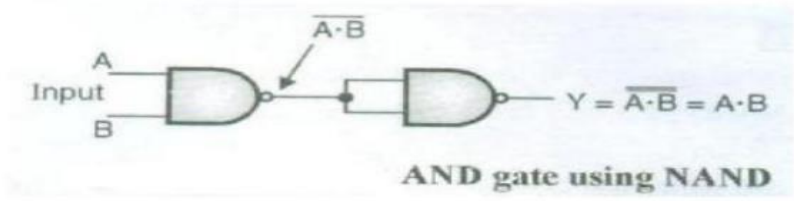
1. PARALLEL LOAD: When mode control (M) is connected to logic 1, AND gates 2, 4, 6, 8 will be enables and AND gates 1, 3,5,7, will be disabled. The 4-bit binary data will be loaded parallel. The clock-2 input will be applied to the flip-flops, since M= 1, AND gates -10 is enabled and gate-9 is disabled. Input will transfer parallel data to QA to QD outputs.

75

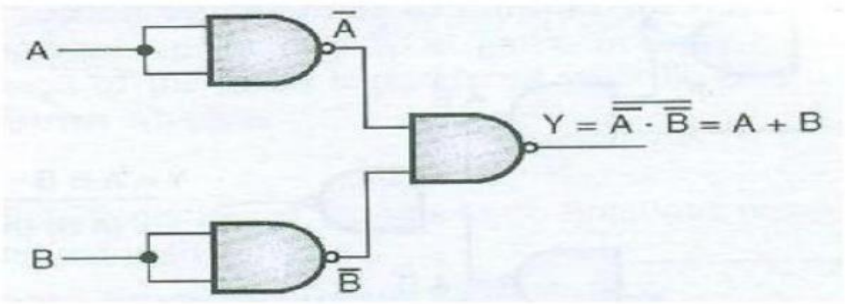
2. SHIFT RIGHT: When mode control (M) is connected to logic 0, AND gates 1,3,5,7 will be enabled and gates 2, 4, 6, 8, will be disabled. The data will be shifted serially. The clock -1, input will be applied to the flip-flops, Since M = 0, AND gates - 9 is enabled, and gates -10 is disabled. The data is shifted serially to right from QA to QD.
3. SHIFT LEFT: When mode control (M) is connected to logic 1, AND gates 2,4,6,8 will be enabled. This mode permits parallel loading of the resister and shift -left operation. The shift -left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip- flop and serial input is applied at the input.

3. Design basic logic gates using NAND and NOR gate.
Ans:

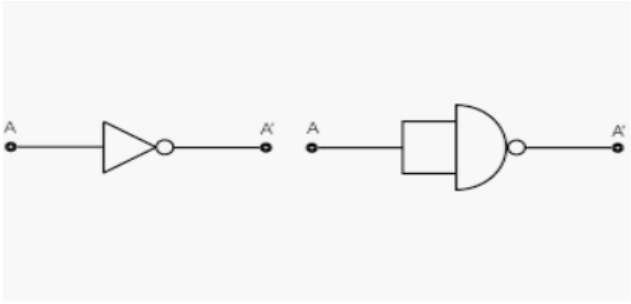
AND gate using NAND



OR gate using NAND

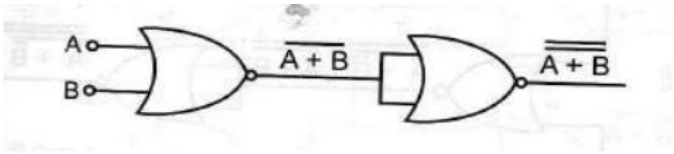


NOT gate using NAND $\overline{A}.\overline{A} = \overline{A}$



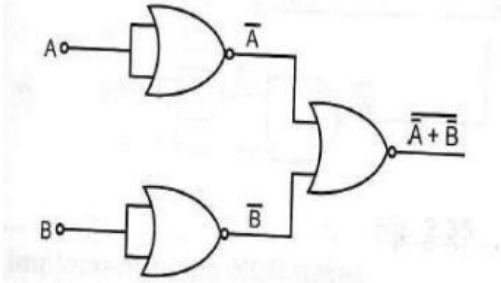
OR gate using NOR gate:
Expression for OR gate is $Y = \overline{\overline{A} + \overline{B}} = A + B$

76

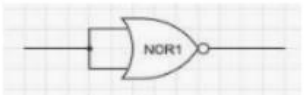


AND gate using NOR gate:

Expression for AND gate is Y = $\overline{\bar{A} + \bar{B}}$ = $\bar{A}.\bar{B}$ = A.B (Applying De Morgan's theorem)



NOT gate using NOR Y= $\overline{A + A}$ = $\bar{A}$



4. Design a mod-6 Asynchronous counter with truth-table and logic.

Ans:

MOD 6 asynchronous counter will require 3 flip flops and will count from 000 to 101. Rest of the states are invalid. To design the combinational circuit of valid states, following truth table and K-map is drawn:

Q_C	Q_B	Q_A	Reset Logic
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

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From the above truth table, we draw the K-maps and get the expression for the MOD 6 asynchronous counter.

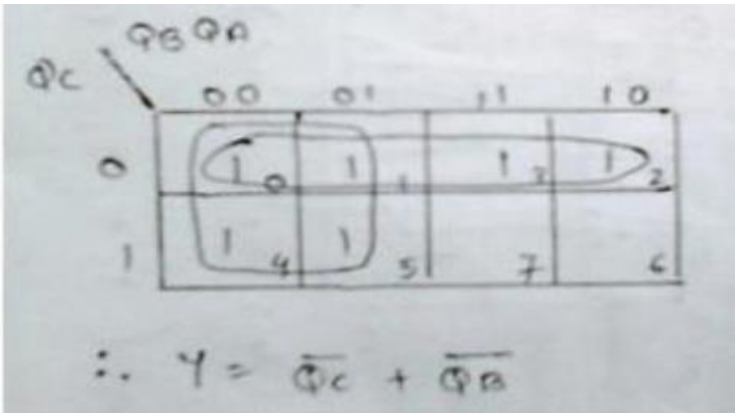

Fig: K-map for above truth table Thus reset logic is OR of complemented forms of QC and QB. This will be given to the reset inputs of the counter so that as soon as count 110 reaches, the counter will reset. Thus, the counter will count from 000 to 101. The implementation of the designed MOD 6 asynchronous counter is shown below:

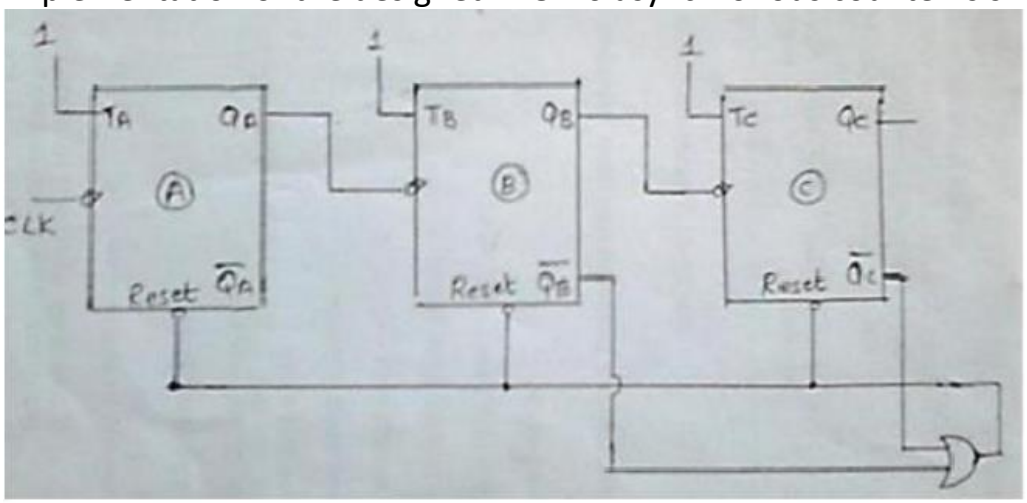

Fig: Circuit diagram of MOD 6 asynchronous counter

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5. Design 1:8 de multiplexer using 1:4 de multiplexer
Ans:

79

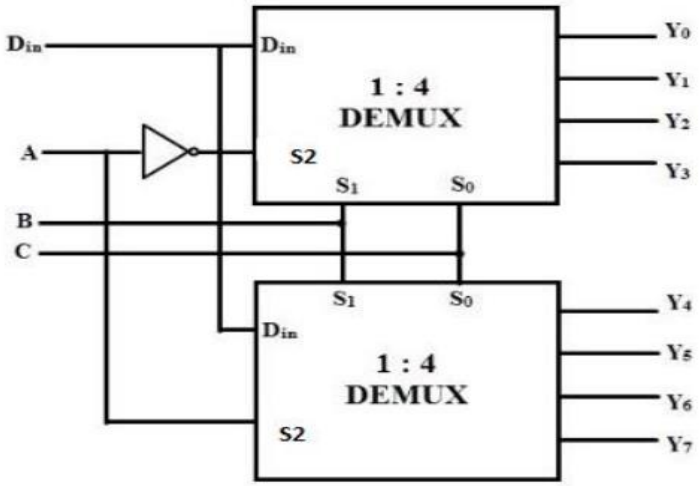


Fig:1:8 Demultiplexer using 1:4 demultiplexer

Data Input	Select Inputs			Outputs							
D	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

6. Draw the circuit diagram of 4-bit R-2R ladder DAC and obtain its output voltage expression

Ans:

80

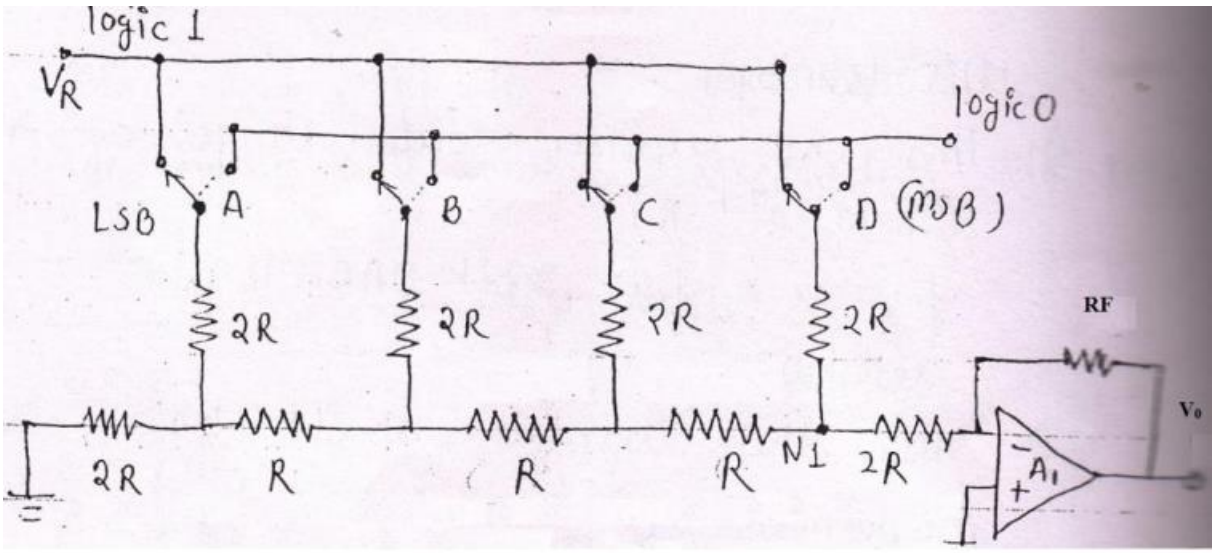


Fig 1: **4 bit R-2R ladder DAC**

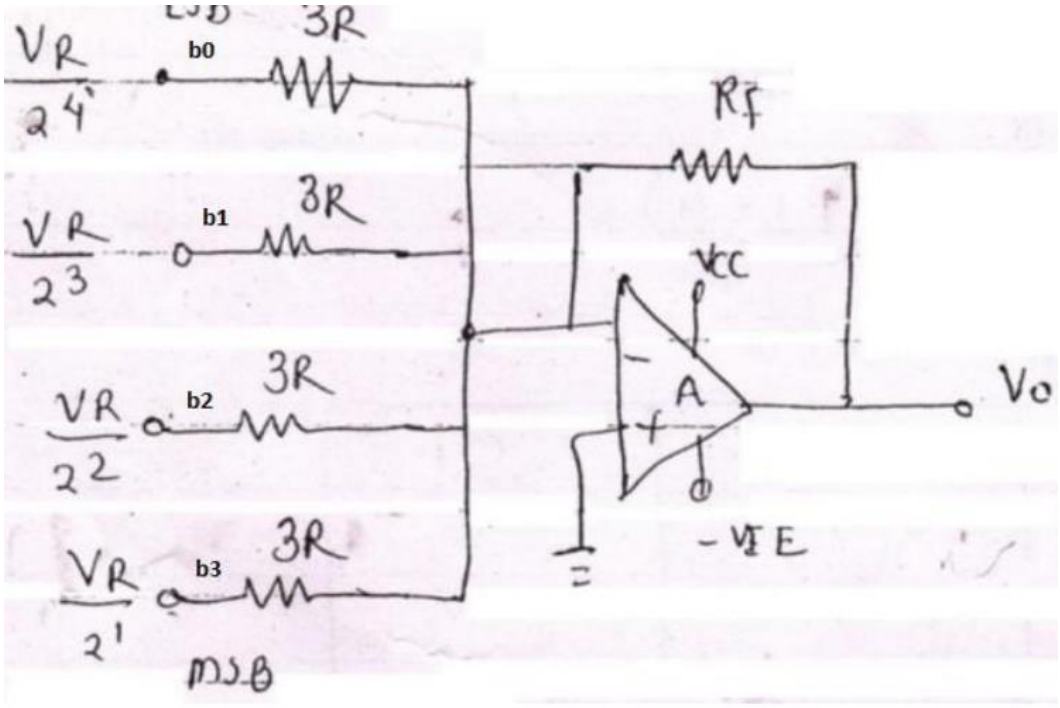


Fig 2:Simplified circuit diagram of Fig 1

Therefore output analog voltage V_0 is given by,

81

$$V_0 = -\left(\frac{Rf}{3R}\cdot\frac{VR}{2^4}b_0 + \frac{Rf}{3R}\cdot\frac{VR}{2^3}b_1 + \frac{Rf}{3R}\cdot\frac{VR}{2^2}b_2 + \frac{Rf}{3R}\cdot\frac{VR}{2^1}b_3\right)$$

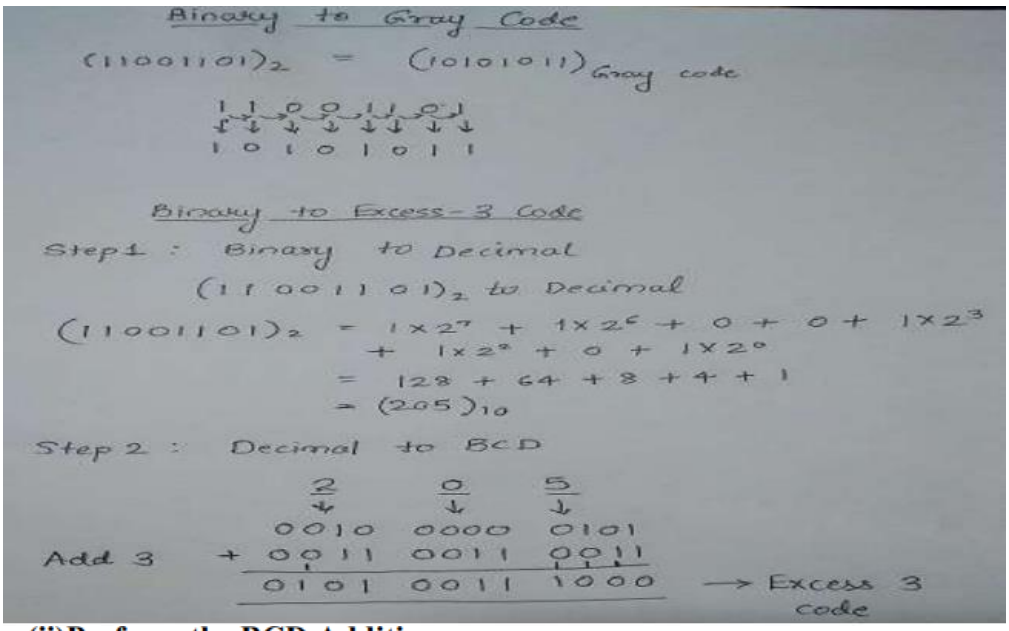
$$V_0 = -\left(\frac{Rf}{3R}\right)\left(\frac{VR}{2^4}\right)[8b_3 + 4b_2 + 2b_1 + b_0]$$

(WINTER-19)

1. **(i)Convert the following binary number $(11001101)_2$ into Gray Code and Excess-3 Code.**

Ans:

82



(ii)Perform the BCD Addition.
$(17)_{10} + (57)_{10}$

Ans:

$(17)_{10}$ 0001 0111
$(57)_{10}$ + 0101 0111 -------(1/2 M)
0110 1110
Valid Invalid
BCD BCD ----------(1/2 M)

ADD 0110 TO Invalid BCD

1 11
0110 1110
+ 0000 0110
01110100 ----------(1/2 M)
7 4
$= (74)_{10}$ ----------(1/2 M)

(iii)Perform the binary addition.
$(10110 \bullet 110)_2 + (1001 \bullet 10)_2$

Ans:

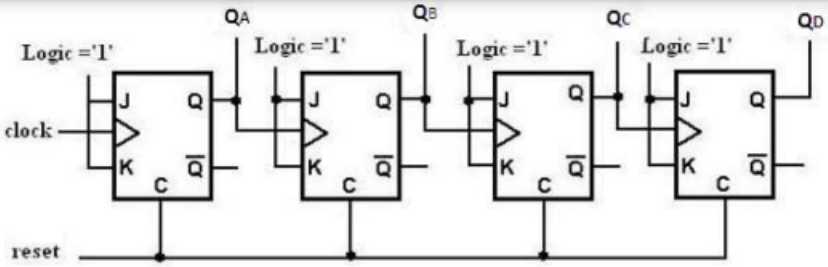
83

$10110.110)_2 - (1001.10)_2 = (100000.010)_2$

```
        11111
        10110.110
+     1001.10
100000.010
```

2. Design a 4bit ripple counter using JK flip flop, with truth table and waveforms.
Ans:

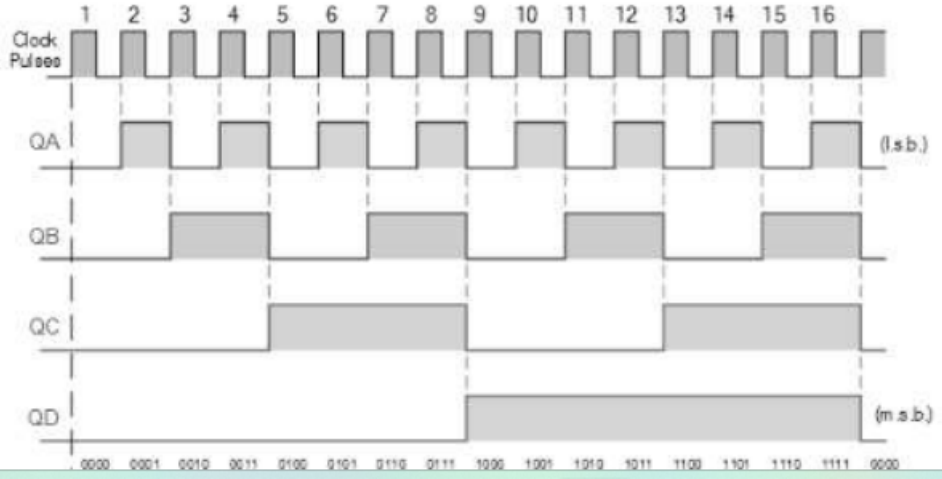
84



Truth Table:

State	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

Timing Diagram / Waveforms:



85

3. **Calculate the analog output for 4 bit weighted register type DAC for inputs**
(i) 1011
(ii) 1001
Assume (V_{fs}) full scale range of voltage is 5V

Ans:

Given:

VR = Vfs = 5V

Formula Used:

$Vo = - VR (B1.2^{-1} + B2.2^{-2} + B3.2^{-3} + B4.2^{-4})$

1. 1011

$Vo = - VR (B1.2^{-1} + B2.2^{-2} + B3.2^{-3} + B4.2^{-4})$

$= - 5 (1*1/2 + 0 + 1*1/2^3 + 1 *1/2^4)$

$= - 5 (1*1/2 + 1*1/8 + 1 *1/16)$

$= - 5 (0.5 + 0.125 + 0.0625) = 3.4375V$

Vo = 3.4375 V

2. 1001

$Vo = - VR (B1.2^{-1} + B2.2^{-2} + B3.2^{-3} + B4.2^{-4})$

$= - 10 (1*1/2 + 0 + 0 + 1 *1/2^4)$

$= - 10 (1*1/2 + 0 + 0 + 1 *1/16)$

$= - 10 (0.5 + 0.0625) = 2.8125V$

Vo = 2.8125 V

---

4. Compare TTL, CMOS and ECL logic family on the following points.
(i) Basic Gates
(ii) Propagation delay
(iii)Fan out
(iv)Power Dissipation
(v) Noise immunity
(vi)Speed power product
Ans:

86

Parameter	TTL	CMOS	ECL
Basic gates	NAND	NOR/NAND	OR/NOR
Propagation delay	10	70-105	2
Fan out	10	50	25
Power Dissipation	10mW	1.01mW	40-55mW
Noise Immunity	0.2V	5V	0.25V
Speed Power Product	100	0.7	100

5. Design a BCD adder using IC 7483.

Ans: **(Note: Labelled combinational circuit can be drawn using universal gate also)**

1) To implement BCD adder, we require:

- 4-bit binary adder for initial addition
- Logic circuit to detect sum greater than 9
- One more 4-bit adder to add 0110201102 in the sum if sum is greater than 9 or carry is 1

2) The logic circuit to detect sum greater than 9 can be determined by simplifying the Boolean expression of given truth Table.

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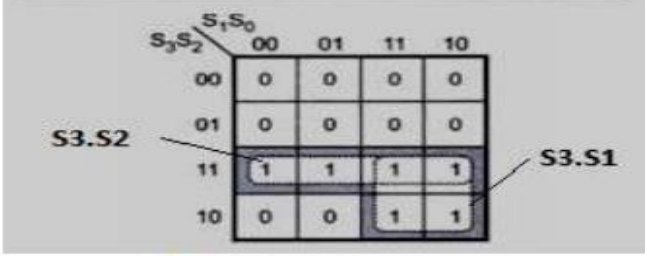
Inputs				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



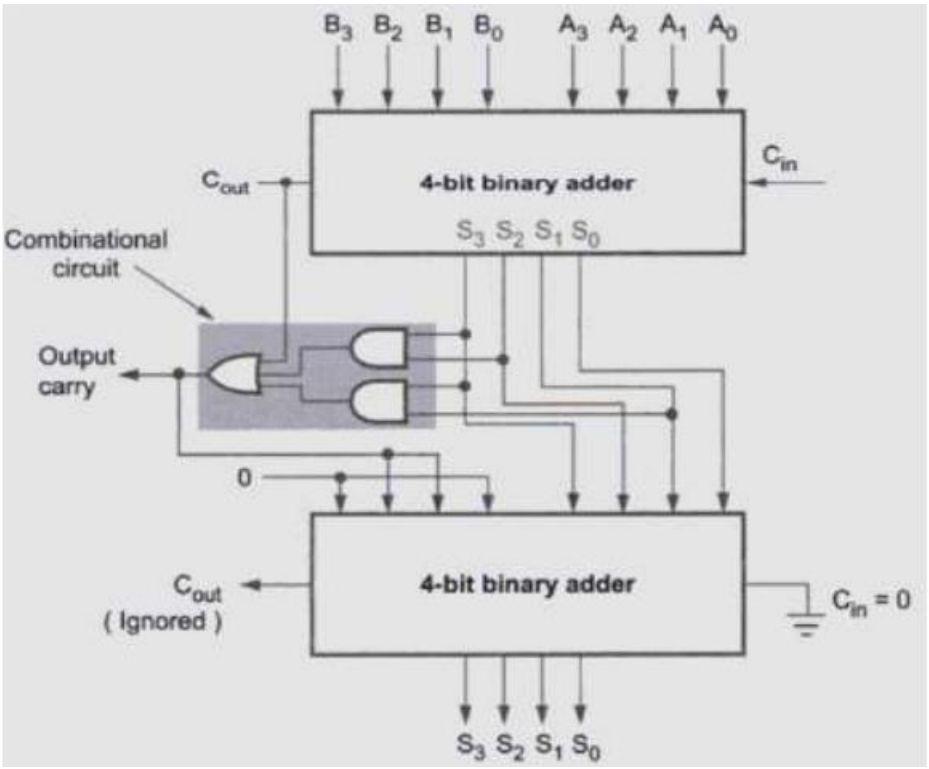
= S3.S2+S3.S1

3) Y=1 indicates sum is greater than 9. We can put one more term, C_out in the above expression to check whether carry is one.

4) If any one condition is satisfied, we add 6(0110) in the sum.

5) With this design information we can draw the block diagram of BCD adder, as shown in figure below.

88



6. Design a 3-bit synchronous counter using JK Flip Flop.

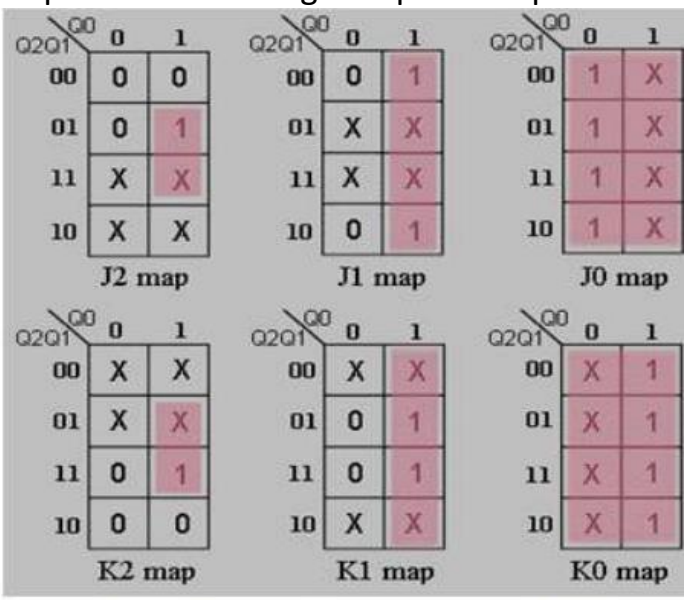
Ans: 1) Step1: Construct JK state table with corresponding excitation table:

89

Output State Transitions				
Present State Q2 Q1 Q0	Next state Q2 Q1 Q0	Flip-flop inputs J2 K2	J1 K1	J0 K0
0 0 0	0 0 1	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 0	1 X	X 1	X 1
1 0 0	1 0 1	X 0	0 X	1 X
1 0 1	1 1 0	X 0	1 X	X 1
1 1 0	1 1 1	X 0	X 0	1 X
1 1 1	0 0 0	X 1	X 1	X 1

State Table and Corresponding Excitation Table (d=don't care)

Step 2: Build Karnaugh Map or Kmap for each JK inputs:

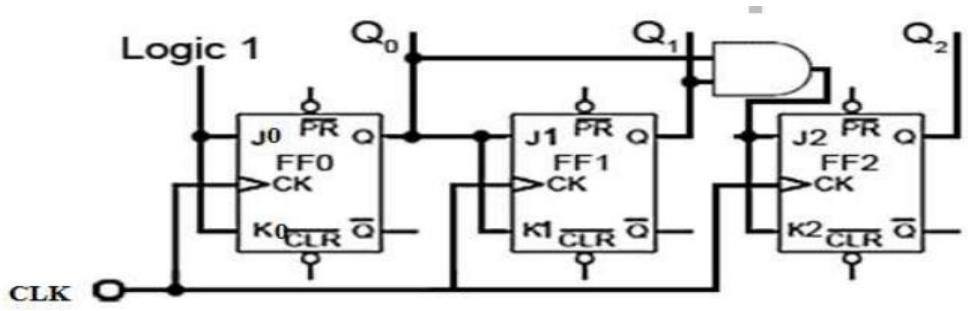


J2=Q1.Q0 **J1=Q0** **J0=1**

K2=Q1.Q0 **K1=Q0** **K=1**

Step3: Draw the complete design as below:

90

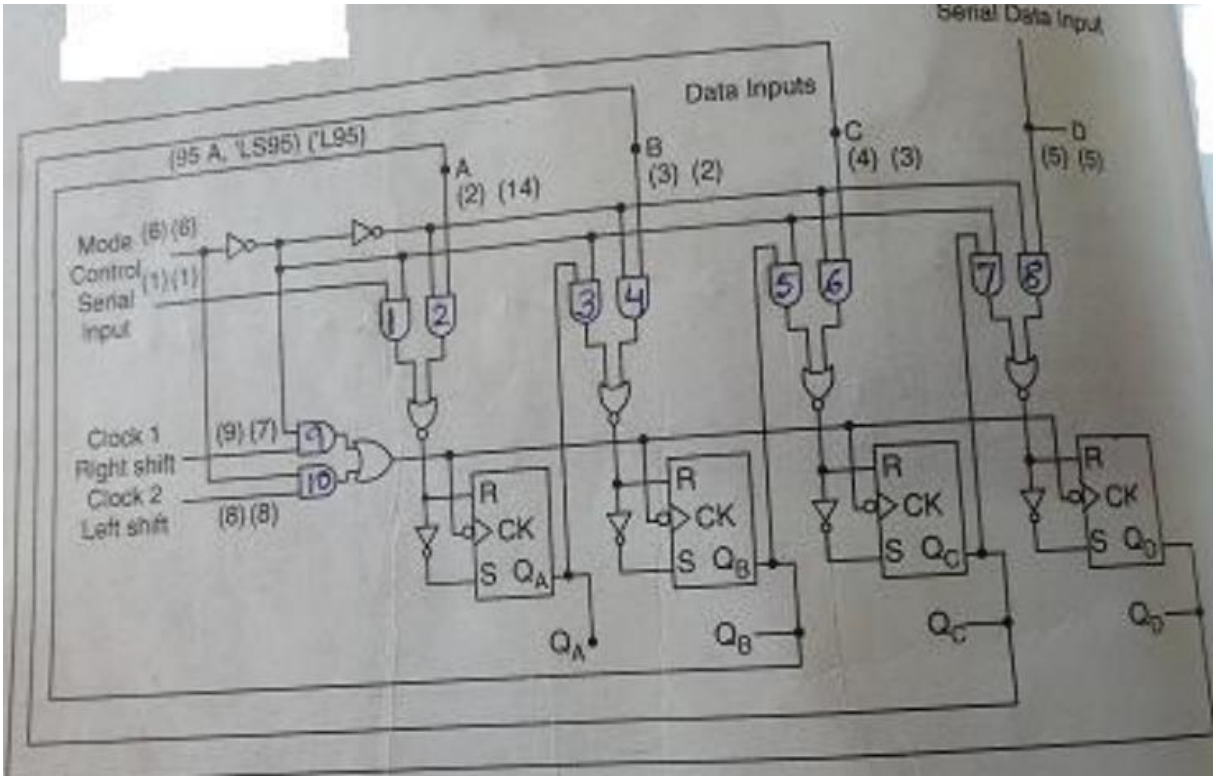


Note: It can also be designed using any other Flip Flop.

(SUMMER-22)

1. Draw and explain operation 4 bit universal shift register. Draw necessary waveforms.

Ans:



Working:

1. PARALLEL LOAD: When mode control (M) is connected to logic 1, AND gates 2, 4, 6, 8 will be enables and AND gates 1, 3,5,7, will be disabled. The 4-bit binary data will be loaded

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parallel. The clock-2 input will be applied to the flip-flops, since M= 1, AND gates -10 is enabled and gate-9 is disabled. Input will transfer parallel data to QA to QD outputs.
2. SHIFT RIGHT: When mode control (M) is connected to logic 0, AND gates 1,3,5,7 will be enabled and gates 2, 4, 6, 8, will be disabled. The data will be shifted serially. The clock -1, input will be applied to the flip-flops, Since M = 0, AND gates - 9 is enabled, and gates -10 is disabled. The data is shifted serially to right from QA to QD.
3. SHIFT LEFT: When mode control (M) is connected to logic 1, AND gates 2,4,6,8 will be enabled. This mode permits parallel loading of the resister and shift -left operation. The shift -left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip- flop and serial input is applied at the input.

2. Draw block diagram of Dual slope ADC and explain its working.
Ans:

92

Principle of Operation:

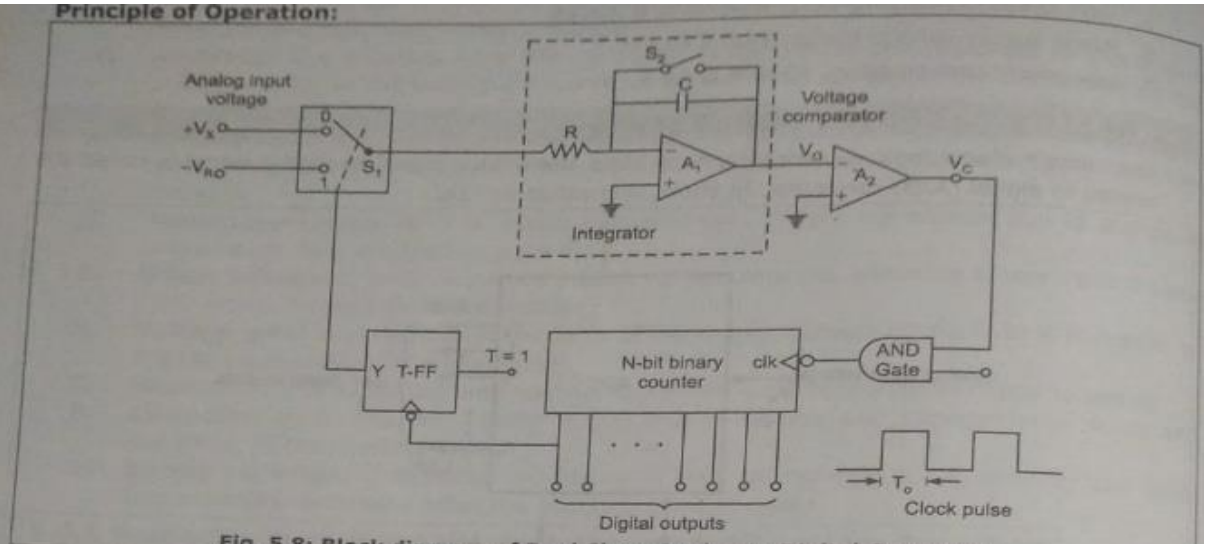

Fig. 5.8: Block diagram of Dual Slope Analog to Digital Converter

- Fig. 5.8 shows the functional block diagram of a Dual-Slope ADC. It consists of four major blocks: 1. an integrator, 2. a comparator, 3. a binary counter and 4. a switch driver, T flip-flop.
- This circuit is provided with a single-pole double throw electronic switch. The initial state of the circuit is such that:
  1. The output of the integrator is small and positive, so that the output of the comparator is low. Thus, the AND gate is disabled.
  2. The counter is kept reset, so that Y output of all flip-flops in the counter are reading 000 ... 00.
  3. The toggle mode flip-flop is kept reset.
- The conversion process begins at t = 0 with the switch S_1 in position 0, thereby connecting the analog voltage V_x to the input of the integrator. The integrator output is:

$$V_o = \frac{-1}{\tau}\int_0^t V_x\,dt = -\left(\frac{V_a}{\tau}\right)t$$

- This results in high V_o, thus enabling the AND gate and the clock pulses reach the clock (clk) input terminal of the counter which was initially clear. The counter counts from 00 ... 00 to 11 ... 111 when $2^N - 1$ clock pulses are applied.
- At the next clock pulse 2^N, the counter is cleared and Q becomes 1. This controls the state of S_1 which now moves to position 1 at T_1, thereby connecting $-V_R$ to the input of the integrator. The

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output of the integrator now starts to move in the positive direction. The counter continues to count until $V_0 < 0$. As soon as V_0 goes positive at T_2, V_c goes low enabling the AND gate. The counter will stop counting in the absence of the clock pulses. The waveforms of voltages V_0 and V_c are shown in Fig. 5.9.

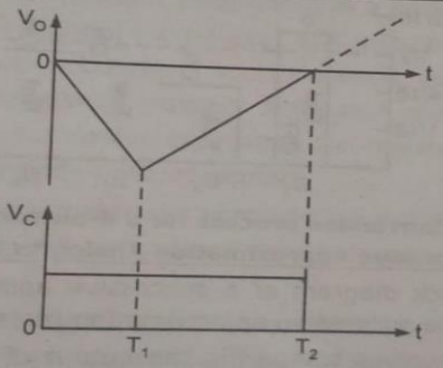

Fig. 5.9: Waveforms of Dual-Slope Analog to Digital Converter

3. Design 16:1 MUX using 4:1 MUX

Ans:

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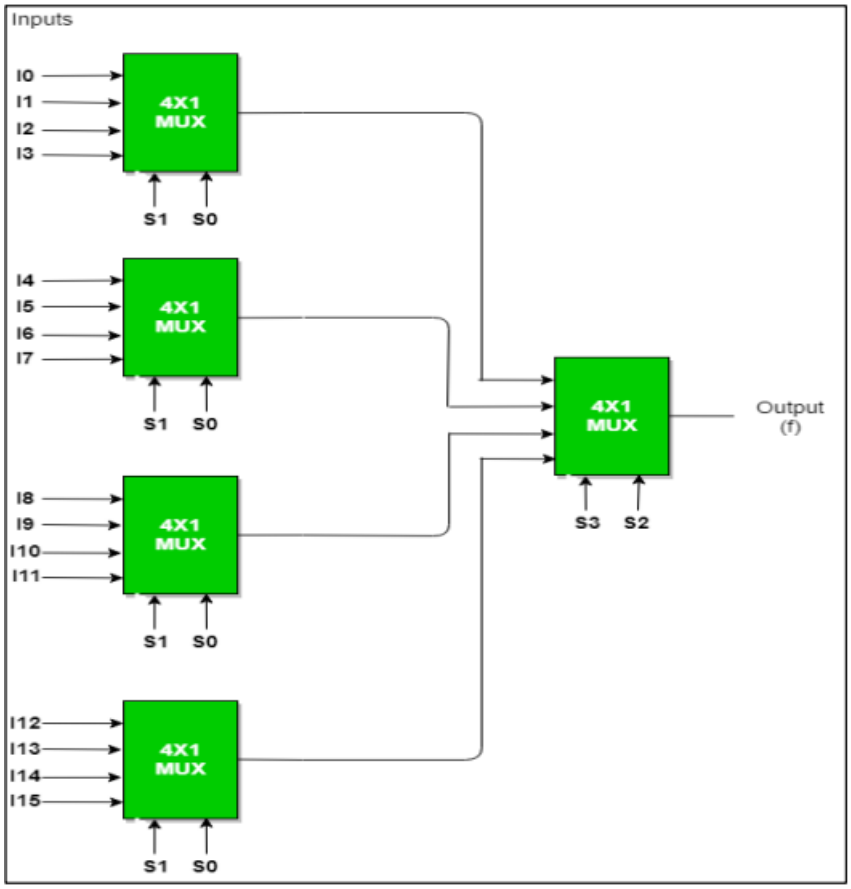

4 . Compare TTL and CMOS with following points. (i) Fan IN (ii) FAN OUT (iii) Propogation delay (iv) Power dissipation

Ans:

Parameter	CMOS	TTL
Propagation delay	70-105 nsec/more than TTL	10 nsec/Less than CMOS
Power Dissipation	Less 0.1 mW/Less than TTL	More 10 mW/ More than CMOS
Fan-out	50/More than TTL	10/Less than CMOS
Basic gate	NAND/NOR	NAND

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(WINTER-22)

1. Explain 3 bit asynchronous counter with output waveforms.

Ans:

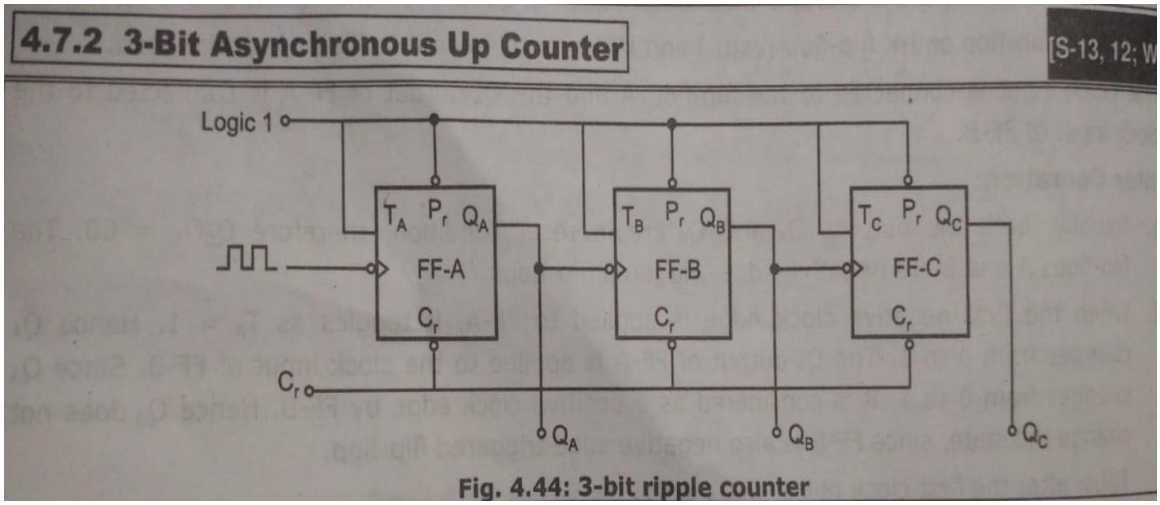

Fig. 4.44: 3-bit ripple counter

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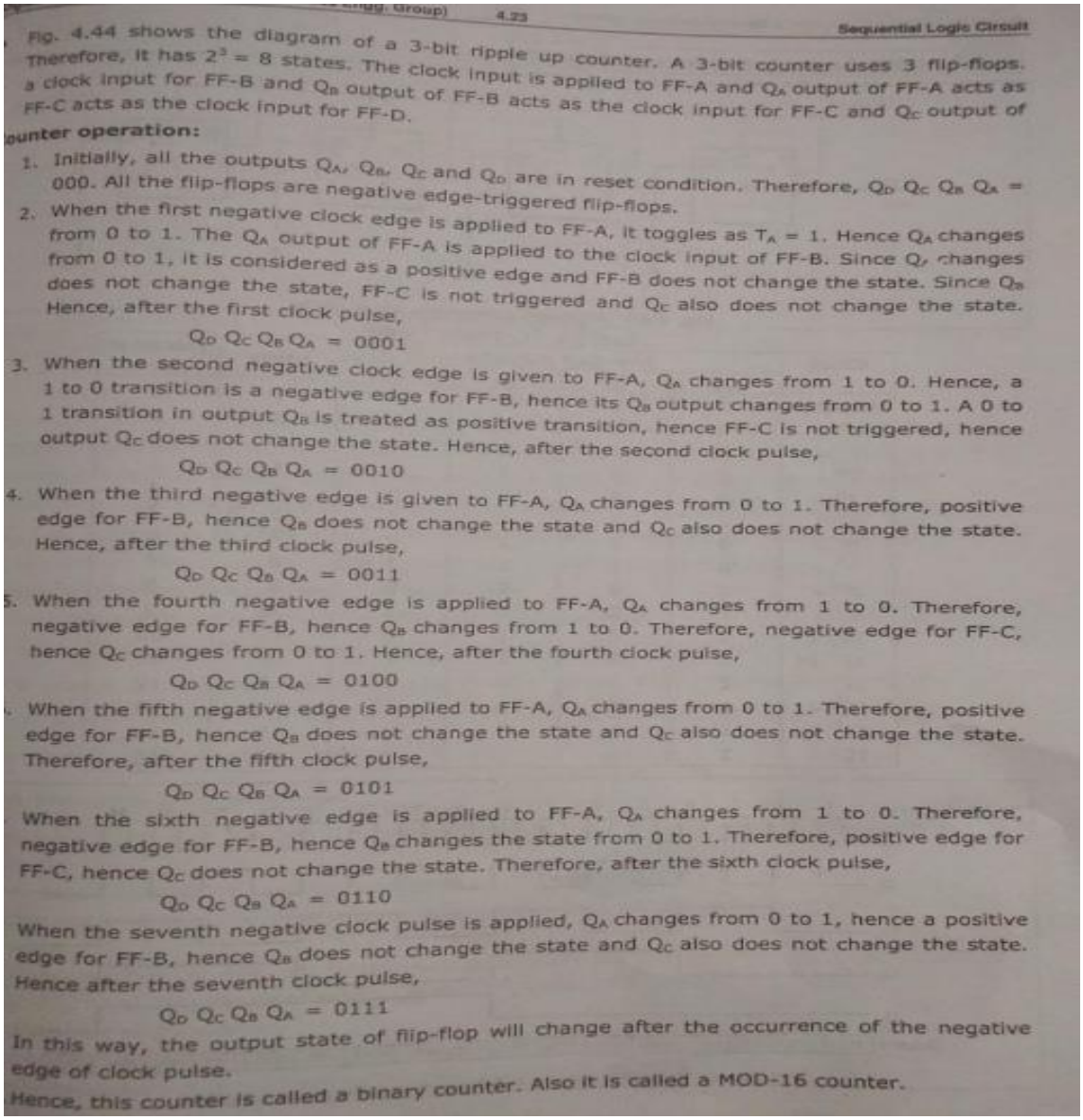

Fig. 4.44 shows the diagram of a 3-bit ripple up counter. A 3-bit counter uses 3 flip-flops. Therefore, it has $2^3 = 8$ states. The clock input is applied to FF-A and Q_A output of FF-A acts as a clock input for FF-B and Q_B output of FF-B acts as the clock input for FF-C and Q_C output of FF-C acts as the clock input for FF-D.

ounter operation:

1. Initially, all the outputs Q_A, Q_B, Q_C and Q_D are in reset condition. Therefore, Q_D Q_C Q_B Q_A = 000. All the flip-flops are negative edge-triggered flip-flops.
2. When the first negative clock edge is applied to FF-A, it toggles as $T_A = 1$. Hence Q_A changes from 0 to 1. The Q_A output of FF-A is applied to the clock input of FF-B. Since Q_A changes from 0 to 1, it is considered as a positive edge and FF-B does not change the state. Since Q_B does not change the state, FF-C is not triggered and Q_C also does not change the state. Hence, after the first clock pulse,

   Q_D Q_C Q_B Q_A = 0001
3. When the second negative clock edge is given to FF-A, Q_A changes from 1 to 0. Hence, a 1 to 0 transition is a negative edge for FF-B, hence its Q_B output changes from 0 to 1. A 0 to 1 transition in output Q_B is treated as positive transition, hence FF-C is not triggered, hence output Q_C does not change the state. Hence, after the second clock pulse,

   Q_D Q_C Q_B Q_A = 0010
4. When the third negative edge is given to FF-A, Q_A changes from 0 to 1. Therefore, positive edge for FF-B, hence Q_B does not change the state and Q_C also does not change the state. Hence, after the third clock pulse,

   Q_D Q_C Q_B Q_A = 0011
5. When the fourth negative edge is applied to FF-A, Q_A changes from 1 to 0. Therefore, negative edge for FF-B, hence Q_B changes from 1 to 0. Therefore, negative edge for FF-C, hence Q_C changes from 0 to 1. Hence, after the fourth clock pulse,

   Q_D Q_C Q_B Q_A = 0100

When the fifth negative edge is applied to FF-A, Q_A changes from 0 to 1. Therefore, positive edge for FF-B, hence Q_B does not change the state and Q_C also does not change the state. Therefore, after the fifth clock pulse,

Q_D Q_C Q_B Q_A = 0101

When the sixth negative edge is applied to FF-A, Q_A changes from 1 to 0. Therefore, negative edge for FF-B, hence Q_B changes the state from 0 to 1. Therefore, positive edge for FF-C, hence Q_C does not change the state. Therefore, after the sixth clock pulse,

Q_D Q_C Q_B Q_A = 0110

When the seventh negative clock pulse is applied, Q_A changes from 0 to 1, hence a positive edge for FF-B, hence Q_B does not change the state and Q_C also does not change the state. Hence after the seventh clock pulse,

Q_D Q_C Q_B Q_A = 0111

In this way, the output state of flip-flop will change after the occurrence of the negative edge of clock pulse.

Hence, this counter is called a binary counter. Also it is called a MOD-16 counter.

2. Compare following (Any three points)

i) RAM with ROM memory.

ii) EPROM with EEPROM memory.

Ans:

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RAM	ROM
1. RAM stands for Random Access Memory.	1. ROM stands for Read Only Memory.
2. Both Read and Write operations can be performed.	2. Only Read operation can be performed.
3. These are volatile memories.	3. These are non-volatile memories.
4. Types: Static RAM and Dynamic RAM.	4. Types: PROM, EPROM, E^2PROM.
5. Applications: Computer, calculator.	5. Applications: Computer, microprocessor.

[W-12]

E^2PROM	EPROM
1. E^2PROM stands for Electrically Erasable Programmable Read Only Memory.	1. EPROM stands for Erasable Programmable Read Only Memory.
2. Can be programmed and erased electrically.	2. Cannot be erased electrically and require UV rays to erase the EPROM.
3. Can be erased in a small time of 10 ms.	3. Requires 20 to 30 min. for erasing the contents.
4. Not required to remove the chip from the circuit for erasing and reprogramming.	4. Chip has to be removed from the circuit for erasing and reprogramming.
5. Low density	5. High density
6. Expensive than EPROM.	6. Cheaper than E^2PROM.

3. Draw the circuit and explain the principle of TTL gate with totempole output
Ans:

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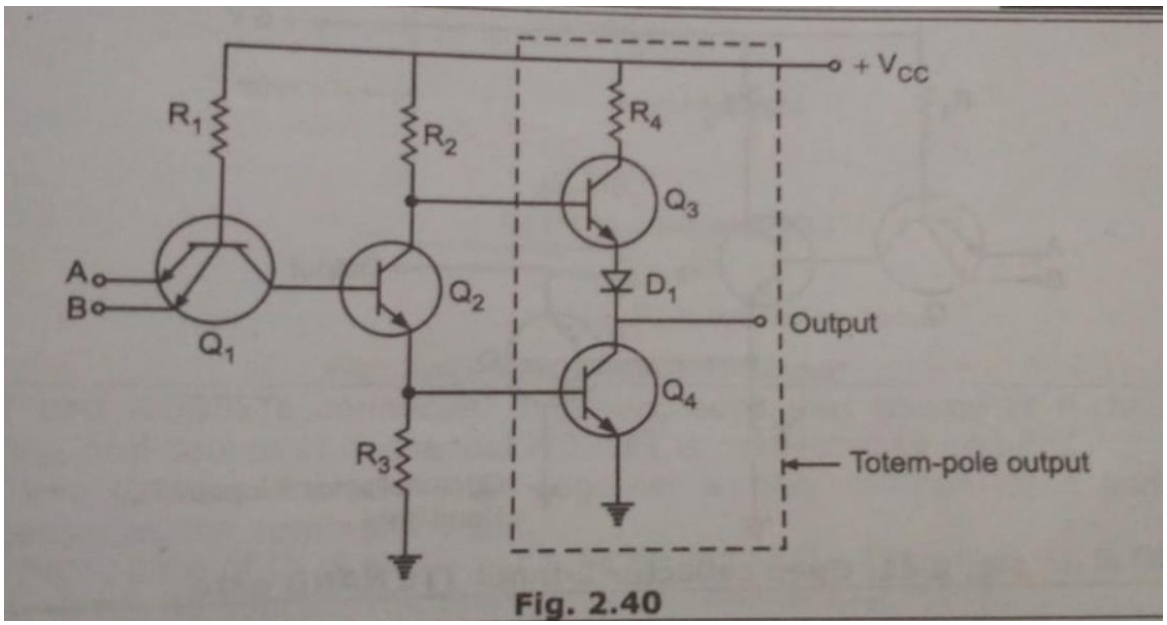

Fig. 2.40

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- Totem-pole transistors are used because they produce a low output. Transistors Q_3 and Q_4 form a totem pole. Either Q_3 acts as an emitter follower or Q_4 is saturated.
- The output impedance is low even when Q_3 is conducting or when Q_4 is saturated.
- The output impedance of gate is not purely resistive but is partially capacitive. The capacitive load is contributed by the output capacitance of the transistor, capacitance of fan-out gates and other wiring stray capacitances. Whenever the output changes from low to high, the output transistor of the gate goes from saturation to cut-off and total load capacitance charges exponentially.
- The totem-pole output reduces propagation delay considerably.
- When output is low, Q_2 and Q_4 are in saturation. Diode D_1 is provided to ensure that Q_3 is cut-off when Q_4 is saturated. As the output changes to a high state the transistors Q_2 and Q_4 go into cut-off region. As soon as Q_2 turns off, Q_3 starts conducting because the base of Q_3 is connected to V_{CC}.
- The high current required to charge the load capacitance causes Q_3 to saturate momentarily and output voltage increases with time constant RC.
- As the load charges, the output voltage rises and current in Q_3 decreases, bringing the transistor into active region. Thus Q_3 is in active region in steady-state condition and output voltage is 3.6 V.

Advantages: [W-12]

1. Provides low output impedance. With output in logic '1' state, Q_3 acts as an emitter follower with its low output impedance drives current into load. This low output impedance gives a short time constant for charging the capacitive load on the output side. Due to this the output voltage can change quickly from one state to another.
2. Low value of circuit power dissipation.

Disadvantages:

1. Wired-logic connection is not allowed with totem-pole output circuits.
2. Totem-pole output circuits generate large current spikes during switching.

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